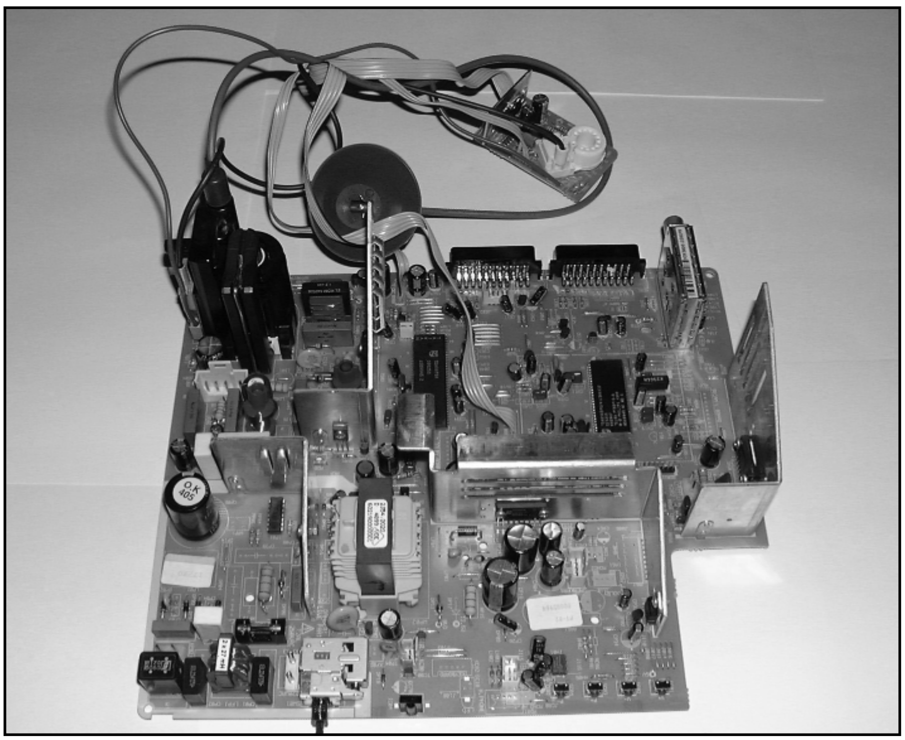
SERVICE MANUAL

PT92 16/9 CHASSIS



CONTENTS

TECHNICAL DATA

CRT PANEL	
Visible Picture	32″ / 106° / 76 cm
Deflection Angle	28″ / 106° / 66 cm.
Vertical Frequency	50Hz
Horizontal Frequency	15.625Hz

ELECTRONIC

Program Number	100+AV
Teletext	Flof text
Tuner	Cable tuner - 8 MHz spacing for Hyper Band
TV System	European CCIR system
Music Power	106° 2x8 Watt Rms 10% distortion

CONNECTIONS

Euro AV Socket	Include

MAIN STAGE

Mains Voltage	165-260VAC
Mains Frequency	50Hz
Power Consumption	28″, 32″ 145 Watt
In Stby Mode	28″, 32″ 11 Watt

RECOMMENDATION FOR SERVICE REPAIRS

1- Use only original spare parts. Only use components with the same specifications for replacement.
2- Original fuse value only should be used.
3- Main leads and connecting leads should be checked for external damage before connection.
   Check the insulation.
4- Parts contributing to the safety of the product must not be damaged or obviously unsuitable.
   This is valid especially for insulators and insulating parts.
5- Thermally loaded solder pads are to be sucked off and re-soldered.
6- Ensure that the ventilation slots are not obstructed.
7- Potentials as high as 25 KV are present when this receiver is operating. Operation of the receiver outside the cabinet or with back cover removed involve a shock hazard from the receiver.
   Servicing should not be attempted by anyone who is not thoroughly familiar with the precautions necessary when working on high voltage equipment.
   Perfectly discharge the high potential of the picture tube before handling the tube. The picture tube is highly evacuated and if broken.
   Glass fragments will be violently expelled.
   Always discharge the picture tube anode to the receiver chassis to keep of the shock hazard before removing the anode cap.
8- Keep wire away from the high voltage or high temperature components.
9- When replacing a wattage resistor in circuit board, keep the resistor 10 mm away from circuit board.

HANDLING OF MOS CHIP COMPONENTS

MOS circuit requires special attention with regard to static charges. Static charges may occur with any highly insulating plastics and can be transferred to persons wearing clothes and shoes made of synthetic materials. Protective circuits on the inputs and outputs of mos circuits give protection to a limited extend only due to time of reaction.

Please observe the following instructions to protect the components against damage from static charges.

1- Keep mos components in conductive package until they are used. Most components must never be stored in styropor materials or plastic magazines.
2- Persons have to rid themselves of electrostatic charges by touching MOS components.
3- Hold the component by the body touching the terminals.
4- Use only grounded instruments for testing and processing purposes.
5- Remove or connect MOS ICs when operating voltage is disconnected.

X-RAY RADIATION PRECAUTION

1- Excessive high voltage can be produce potentially hazardous X-RAY radiation. To avoid such hazard, the high voltage must not be above the specified limit. The nominal value of the high voltage of this receiver is 25KV at zero beam current (minimum brightness) under 220V AC power source. The high voltage must not under any circumstance, exceed 30KV. It is recommended the reading of the high voltage be recorded as a part of the service record. It is important to use an accurate and reliable high voltage meter.
2- The primary source of X-RAY radiation in this TV receiver is the picture tube. For continued X-RAY radiation protection, the replacement tube must be exactly the same type tube as specified in the part list.

SERVICE MENU

The service menu is entered by pressing the <SUB-PAGE> key on the RC and VOLUME-DOWN key on the TV simultaneously when the TV is in TV- mode. The service menu is left by pressing the <TV> key.

When entering the service mode the first menu item is IF (selection of normal IF). Next items can be selected using the keys <PROGRAM-UP> and <PROGRAM-DOWN>. The value of each item can be changed using the keys <VOLUME-UP> and <VOLUME-DOWN>. The item values are displayed as decimal values, except for the tuner-band-selection, BITS and option items.

They are displayed as hexa-decimal values. All values are stored in non-volatile memory when the service menu is left. The "INIT CTV832U" item initializes the NVM: It clears all names and tuning information of all programs and writes default values for the service alignments and preset values in NVM. While doing so, the OSD displays "BUSY". When the initialization is finished, the message "READY" is written on the screen.

Item	Default	Explanation
IF	38.9	IF selection (58.8, 45.8, 38.9 or 38.00 MHz)
IFL1	33.9	IF for SECAM-L1 selection (33.4 or 33.9 MHz)
HP	31	Horizontal parallelogram
HB	31	Horizontal bow
EW	37	East-west Width for picture setting 16:9
PW	18	East-west Parabola for picture setting 16:9
UCP	13	East-west Upper Corner parabola for picture setting 16:9
LCP	13	East-west Lower Corner parabola for picture setting 16:9
TC	28	East-west Trapezium for picture setting 16:9
HP4:3	31	Horizontal parallelogram for picture setting 4:3
HB4:3	31	Horizontal bow for picture setting 4:3
EW4:3	45	East-west Width for picture setting 4:3
PW4:3	15	East-west Parabola for picture setting 4:3
UCP4:3	35	East-west Upper Corner parabola for picture setting 4:3
LCP4:3	25	East-west Lower Corner parabola for picture setting 4:3
TC4:3	31	East-west Trapezium for picture setting 4:3
HS	31	Horizontal Shift
VS	31	Vertical Slope
VA	31	Vertical Amplitude
SC	31	S-Correction
VSD	off	Vertical Scan Disable
VSH	31	Vertical Shift
VX	25	Vertical zoom (East-west only)
BLR	7	Black Level Red
BLG	7	Black Level Green
WPR	31	White point correction Red
WPG	31	White point correction Green
WPB	31	White point correction Blue
Ys	15	Y-delay adjustment for SECAM
Yn	8	Y-delay adjustment for NTSC
YP	0	Y-delay adjustment for PAL

Yo	0	Y-delay adjustment for external sources
AGC	4	AGC take over
CL	4	Cathode drive level
Bits	00	(ACL=0; FCO= 0; SVO= 0; HP2= 0; FSL= 0; OSO= 0)
Bits1	00	(FFI= 0; TV= 0; AV-1= 0; AV-2= 0; AV-2S= 0; AV-3= 0; AV-3S= 0; AV = 0)

OptByte1 **(Default=E3)**

PAL-BG	=	Selection PAL-BG	(1)
PAL-DK	=	Selection PAL-DK	(1)
PAL-I	=	Selection PAL-I	(0)
PAL-M	=	Selection PAL-M	(0)
PAL-N	=	Selection PAL-N	(0)
NTSC-M	=	Selection NTSC-M	(1)
NTSC-443	=	Selection NTSC-443	(1)
SECAM-BG	=	Selection SECAM-BG	(1)

*(1) Selected, (0) Not Selected

OptByte2 **(Default=07)**

SECAM-DK	=	Selection SECAM-DK	(1)
FRANCE	=	Selection FRANCE	(1)
WEB	=	Enable/Disable	(1/0)
PalBG Scr	=	When the PalBG Scr selected, TV searches only PalBG. Otherwise it searches all.	(0)
AV2	=	Selection AV2	(0)

*(1) Selected, (0) Not Selected

OptByte3 **(Default=E8)**

	=	(0)
JR	=	(0)
HP	=	(0)
Vol Bar	=	(1)
Sub Wof	=	(0)
Presets	=	(1)
Lock	=	(1)
Hotel	=	(0)

When the Hotel mode selected, It's impossible to
nter menu settings.It selects the Hotel mode. (1)

*(1) Selected, (0) Not Selected

OptByte4 **(Default=B8)**

16:9	=	Set 16:9 mode active	(1)
110	=	Selection 110/90 Tube	(1/0)
Hpol	=	Default	(0)
Vpol	=	Default	(0)
Field	=	Default	(1)
FE-Out	=	Default	(1)
Sw-on	=	When the power on the TV, it Enables or Disables Standby Mode.	(1/0)
Vg-Check	=	Default	(1)

*(1) Selected, (0) Not Selected

OptByte5 **(Default=09)**

Clock	=	Enable/Disable Clock Menu	(1)
AM/PM	=		(1)
AVL	=	Auto Volume Level	(1)
	=		(0)
1-norma	=	Default	(0)
Flof-Txt	=		(0)
TR	=		(0)
DVD Start	=		(0)

*(1) Selected, (0) Not Selected

OptByte6			**(Default=00)**
UOC-J	=	Default	(0)
ignrSUP	=	Default	(0)
ignrNDF	=	Default	(0)
Pal-BG/DK	=		(0)
Pal-L	=		(0)
Eco	=		(0)
WEB ST	=		(0)
WSS	=		(0)

TSL	45	Start frequency of the low-band in MHz
TEL	118	End frequency of the low-band
TSM	118	Start frequency of the mid-band
TEM	400	End frequency of the mid-band
TSH	400	Start frequency of the high-band
TEH	863	End frequency of the high-band
TBL	03	hex Value needed for switching to the low-band
TBN	06	hex Value needed for switching to the mid-band
TBH	85	hex Value needed for switching to the high-band

16:9 / 4:3 Adjustment

The CTV832U software uses two sets of parameters for the registers HP (horizontal parallelogram), HB (horizontal bow), EW (EW width), PW (parabola/width), UCP (upper corner parabola), LCP (lower corner parabola) and IC (EW trapezium). They occur in the service menu for 16:9 screen with the listed abbreviations.

For the 4:3 screen there is a second set of these registers. They occur in the service menu with the extension ‘4:3’ (i.e. HP4:3, HB4:3,...).

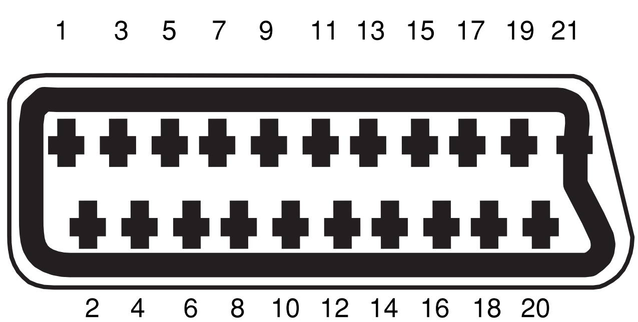
Each register set must be adjusted under the right conditions i.e. the 16:9 settings are adjusted with a 16:9 picture - the 4:3 settings with a 4:3 picture.

The inenu items EW, PW, UCP, LCP, TC, HP4:3, HB4:3,... TC4:3 and VX will only be in the service menu if the option 16:9 is set in 4 th option byte.

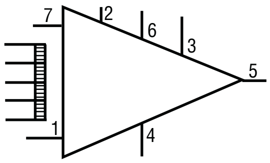
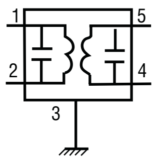
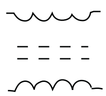
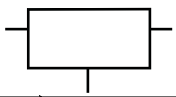
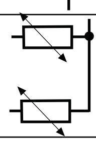
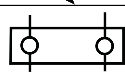
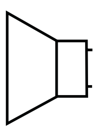
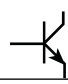
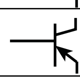
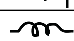
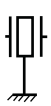
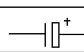
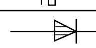
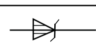
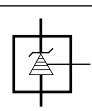
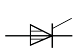
TUNER PARAMETER IN SERVICE AND DEFINITION		PHILIPS	OREGA	TEMIC	SAMSUNG	ALPS
TSL	Start frequency of the low-band in MHz	45	45	45	45	45
TEL	End frequency of the low-band	160	118	150	150	180
TSM	Start frequency of the mid-band	160	118	150	150	180
TEM	End frequency of the mid-band	440	400	440	425	465
TSH	Start frequency of the high-band	440	400	440	425	465
TEH	End frequency of the high-band	863	865	865	865	900
TBL	hex Value needed for switching to the low-band	A1	03	01	01	01
TBN	hex Value needed for switching to the mid-band	92	06	02	02	02
TBH	hex Value needed for switching to the high-band	34	85	04	08	0C

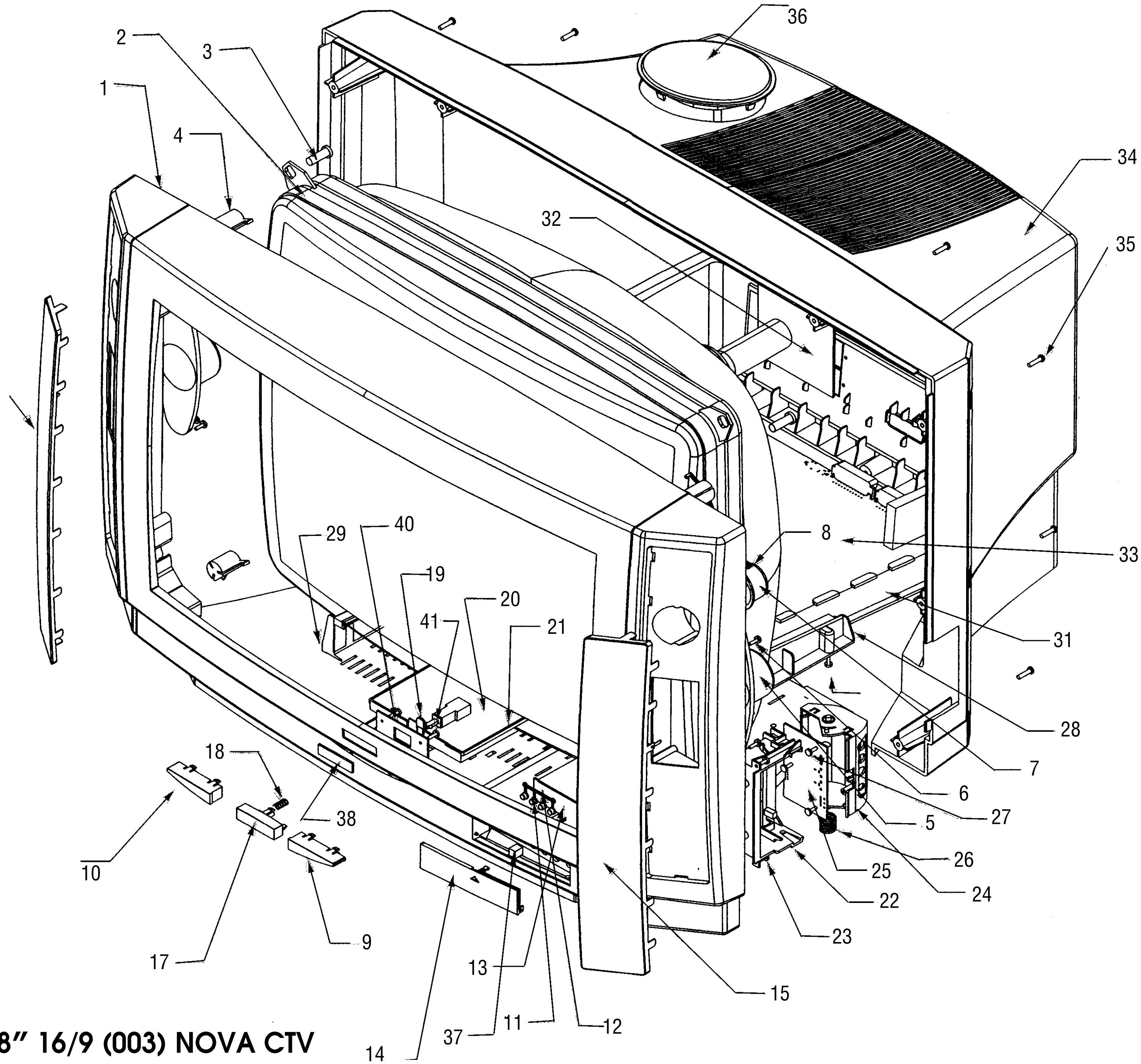
SPECIFICATIONS OF THE CONNECTOR
(EURO SCART)

I- Audio output 1. right channel 0.5 VRMS/<l k 0
2- Audio input 1. right channel 0.5 VRMS (connected to No.6)
3- Audio output 2. left channel 0.5 VRMS (connected to No.1)
4- GND (audio)
5- GND
6- Audio input 2. left channel 0.5 VRMS/>10k 0
7- RGB input, blue (B)
8- Switch signal video (status)
9- GND
10- Reserved for clock signals (not connected)
11- RGB input, green (G)
12- Reserved for remote control (not connected)
13- GND
14- GND switch signal RGB
15- RGB input, red (R)
16- Switch signal RGB
17- GND (video)
18- GND19- Video output 1 Vpp/75 ohm
20- Video input 1 Vpp/75 ohm
21- Shield



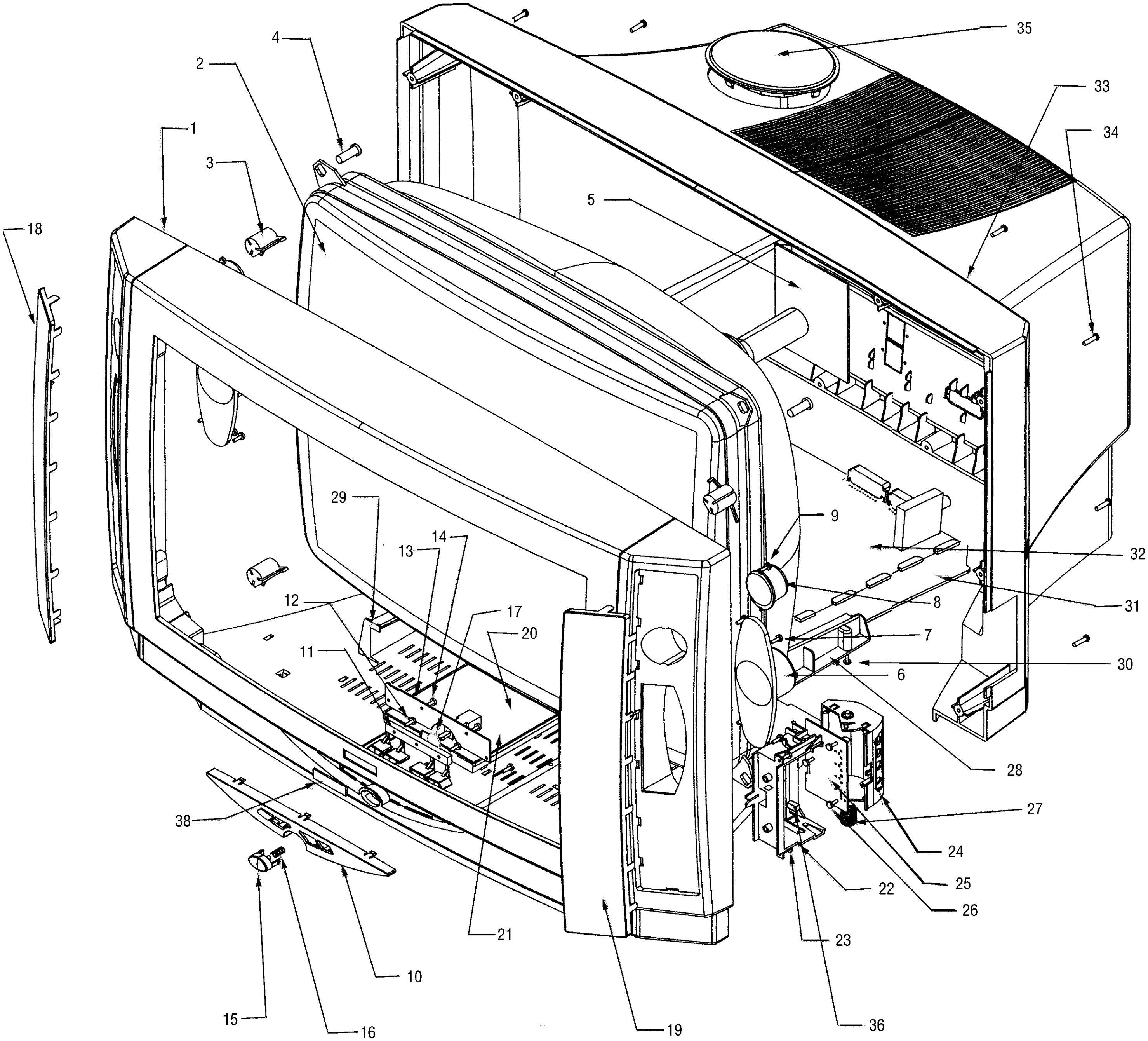
COMPONENT DESCRIPTIONS

	POWER AMPLIFIER
	SAW FILTER
	LINE FILTER
	VOLTAGE REGULATOR
	PTC
	CONNECTOR
	LOUD-SPEAKER
	NPN TRANSISTOR
	PNP TRANSISTOR
	COIL
	LINEARITY COIL
	CERAMIC FILTER
	RESISTOR
	CERAMIC CAPACITOR /POLYESTER CAPACITOR
	ELECTROLYTIC CAPACITOR
	DIODE
	ZENER DIODE
	PROGRAMMABLE VOLTAGE REFERENCE
	THYRISTOR



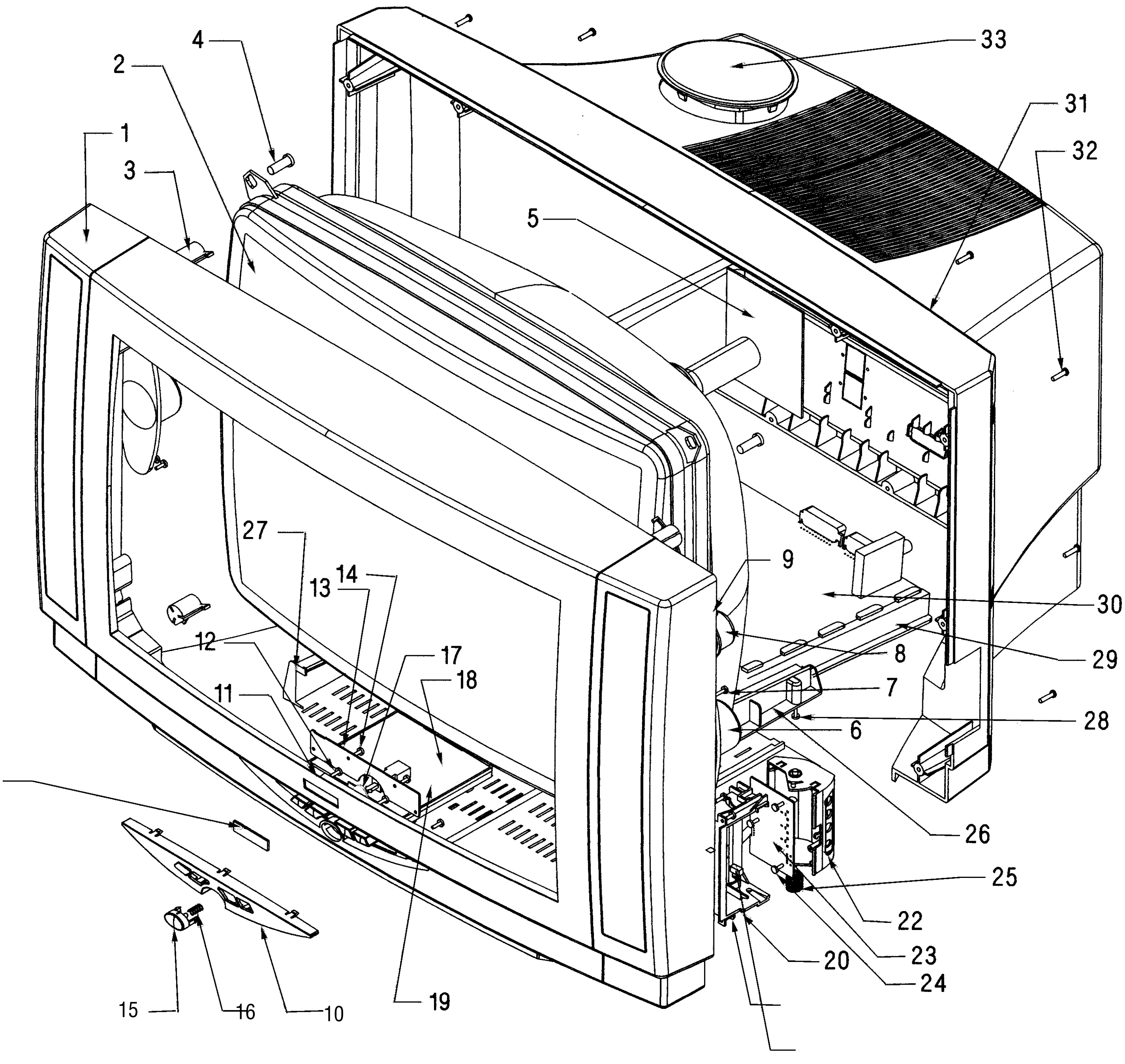
8″ 16/9 (003) NOVA CTV

1- 28″ 16/9 003 FRONT CABINET
2- 28″ 16/9 CRT
3- 28″ 16/9 CRT SCREW Ø 10x40
4- CRT INSERT
5- SPEAKER
6- SPEAKER SCREW Ø 3.9x13
7- TWEETER
8- TWEETER SCREW Ø 2.9x9.5
9- ACYRILIC WINDOW RIGHT (003)
10- ACYRILIC WINDOW LEFT (003)
11- MULTIBUTON (003)
12- REMOTE PCB
13- MULTIBUTON PCB SCREW Ø 2.9x6.5
14- CONTROL DOOR
15- SPEAKER GRILL RIGHT
16- SPEAKER GRILL LEFT
17- ON-OFF BUTON
18- ON-OFF BUTON SPRING
19- ON-OFF BUTON HOLDER
20- ON-OFF PCB
21- ON-OFF PCB HOLDER
22- AV HOLDER 1
23- AV HOLDER SCREW Ø 2.9x13
24- AV HOLDER 2
25- AV PCB
26- AV HOLDER SPRING
27- AV PCB SCREW Ø 2.9x6.5
28- CHASSIS RAIL RIGHT
29- CHASSIS RAIL LEFT
30- CHASSIS RAIL SCREW Ø 3.9x9.5
31- FRAME MAIN PCB
32- CRT PCB
33- MAIN PCB
34- BACK COWER
35- BACK COWER SCREW Ø 3.9x19
36- HORN DOOR
37- DOOR LOCK
38- LOGO
39- 28″ 16/9 STYROPHOR
40- LED PCB
41- LED PCB SCREW Ø 2.9x6.5



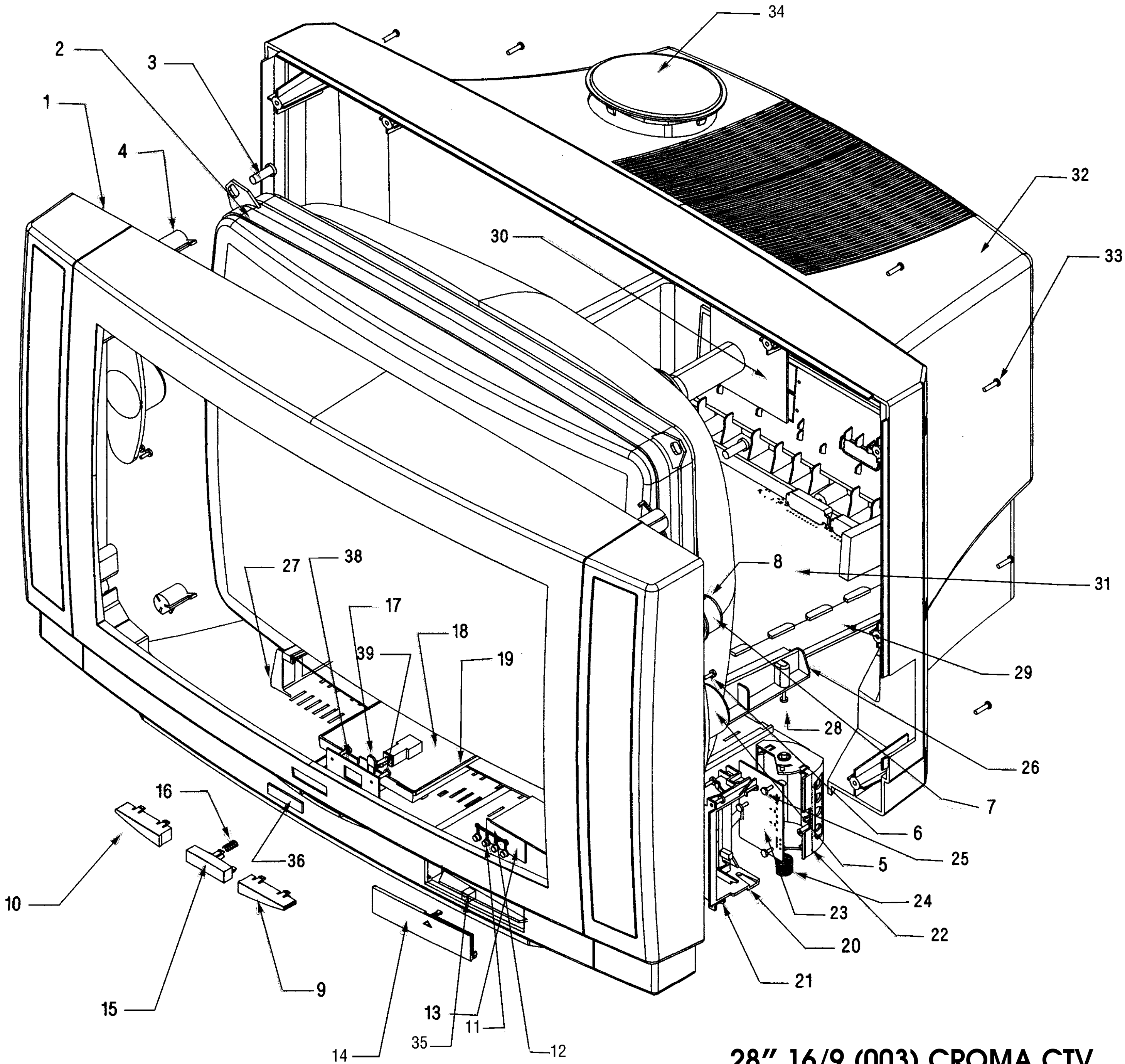
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5- CRT PCB
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7- SPEAKER SCREW Ø 3.9x13
8- TWEETER
9- TWEETER SCREW Ø 2.9x9.5
10- ACYRILIC WINDOW (001)
11- MULTIBUTON (001)
12- MULTIBUTON PCB SCREW Ø 2.9x9.5
13- REMOTE PCB
14- REMOTE PCB SCREW Ø 2.9x6.5
15- ON-OFF BUTON
16- ON-OFF BUTON SPRING
17- ON-OFF HAT
18- SPEAKER GRIL LEFT
19- SPEAKER GRIL RIGHT
20- ON-OFF PCB
21- ON-OFF PCB HOLDER
22- AV HOLDER 1
23- AV HOLDER SCREW Ø 2.9x13
24- AV HOLDER 2
25- AV PCB
26- AV PCB SCREW Ø 2.9x6.5
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28- CHASSIS RAIL RIGHT
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32- MAIN PCB
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34- BACK COWER SCREW Ø 3.9x19
35- HORN DOOR
36- DOOR LOCK
37- 28″ 16/9 NOVA STYROPHOR
38- LOGO

28″ 16/9 (001) NOVA CTV



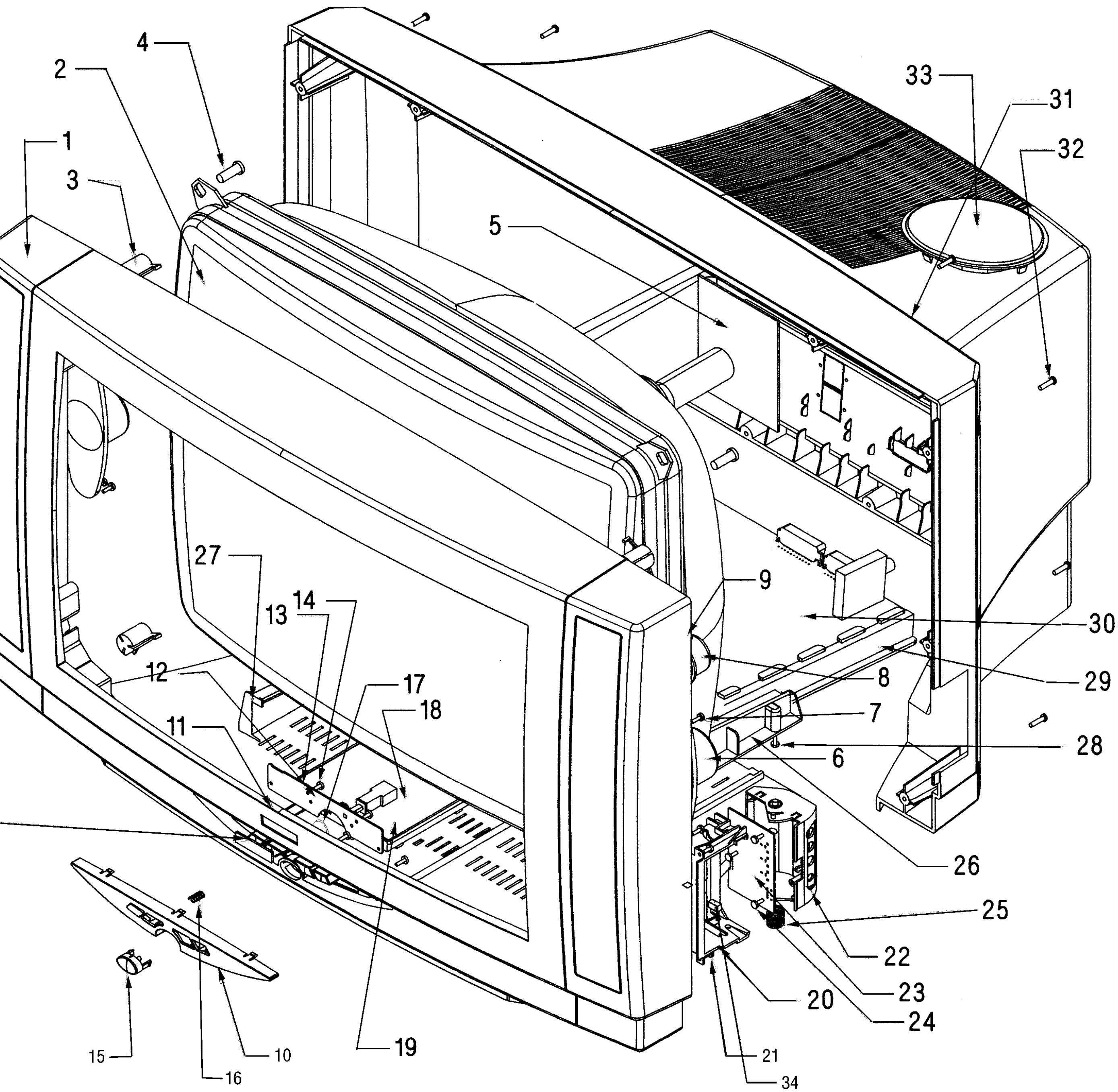
28″ 16/9 (001) CROMA CTV

1- 28″ 16/9 001 FRONT CABINET
2- 28″ 16/9 CRT
3- CRT INSERT
4- 28″ 16/9 CRT SCREW Ø 10x40
5- CRT PCB
6- SPEAKER
7- SPEAKER SCREW Ø 3.9x13
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9- TWEETER SCREW Ø 2.9x9.5
10- ACYRILIC WINDOW (001)
11- MULTIBUTON (001)
12- MULTIBUTON PCB SCREW Ø 2.9x9.5
13- REMOTE PCB
14- REMOTE PCB SCREW Ø 2.9x6.5
15- ON-OFF BUTON
16- ON-OFF BUTON SPRING
17- ON-OFF HAT
18- ON-OFF PCB
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20- AV HOLDER 1
21- AV HOLDER SCREW Ø 2.9x13
22- AV HOLDER 2
23- AV PCB
24- AV PCB SCREW Ø 2.9x6.5
25- AV HOLDER SPRING
26- CHASSIS RAIL RIGHT
27- CHASSIS RAIL LEFT
28- CHASSIS RAIL SCREW Ø 3.9x9.5
29- FRAME MAIN PCB
30- MAIN PCB
31- BACK COWER
32- BACK COWER SCREW Ø 3.9x19
33- HORN DOOR
34- DOOR LOCK
35- 28″ 16/9 NOVA STYROPHOR
36- LOGO
37-
38-



28″ 16/9 (003) CROMA CTV

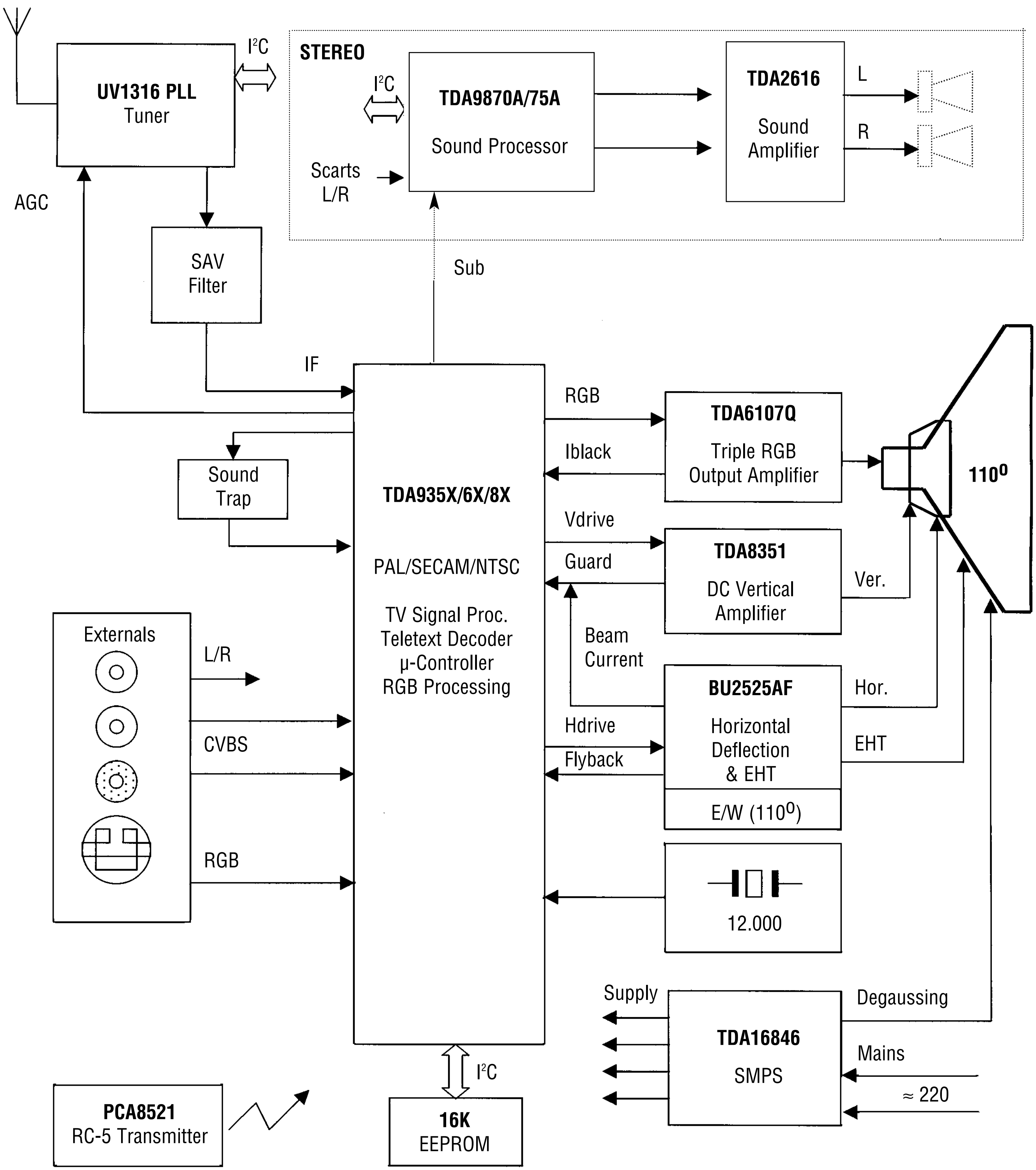
1- 28″ 16/9 003 FRONT CABINET
2- 28″ 16/9 CRT
3- 28″ 16/9 CRT SCREW Ø 10x40
4- CRT INSERT
5- SPEAKER
6- SPEAKER SCREW Ø 3.9x13
7- TWEETER
8- TWEETER SCREW Ø 2.9x9.5
9- ACYRILIC WINDOW RIGHT (003)
10- ACYRILIC WINDOW LEFT (003)
11- MULTIBUTON (003)
12- REMOTE PCB
13- MULTIBUTON PCB SCREW Ø 2.9x6.5
14- CONTROL DOOR
15- ON-OFF BUTON
16- ON-OFF BUTON SPRING
17- ON-OFF BUTON HOLDER
18- ON-OFF PCB
19- ON-OFF PCB HOLDER
20- AV HOLDER 1
21- AV HOLDER SCREW Ø 2.9x13
22- AV HOLDER 2
23- AV PCB
24- AV HOLDER SPRING
25- AV PCB SCREW Ø 2.9x6.5
26- CHASSIS RAIL RIGHT
27- CHASSIS RAIL LEFT
28- CHASSIS RAIL SCREW Ø 3.9x9.5
29- FRAME MAIN PCB
30- CRT PCB
31- MAIN PCB
32- BACK COWER
33- BACK COWER SCREW Ø 3.9x19
34- HORN DOOR
35- DOOR LOCK
36- LOGO
37- 28″ 16/9 STYROPHOR
38- LED PCB
39- LED PCB SCREW Ø 2.9x6.5



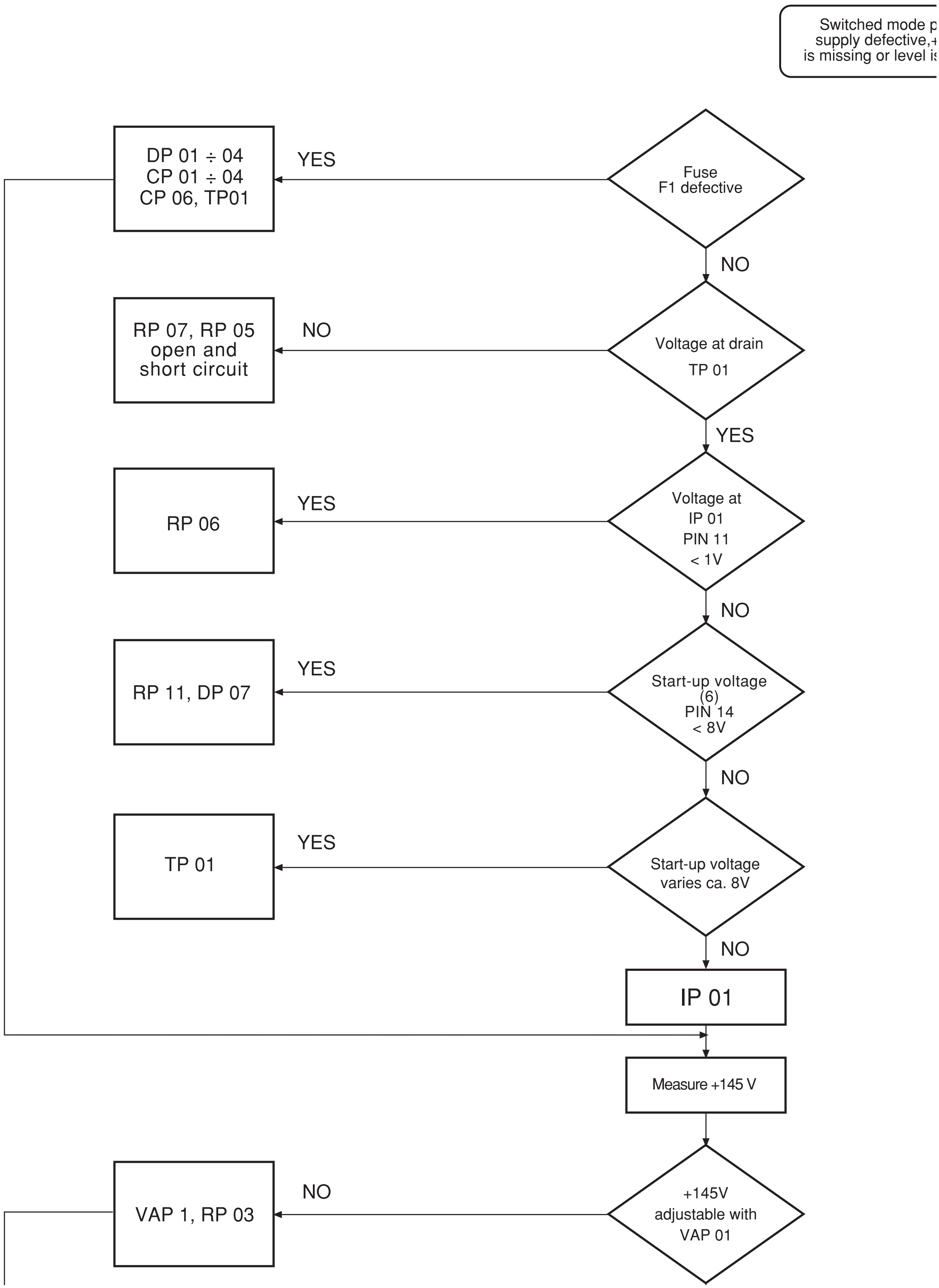
32" 16/9 (001) CROMA CTV

1- 32" 16/9 001 FRONT CABINET
2- 32" 16/9 CRT
3- CRT INSERT
4- 32" 16/9 CRT SCREW Ø 10x40
5- CRT PCB
6- SPEAKER
7- SPEAKER SCREW Ø 3.9x13
8- TWEETER
9- TWEETER SCREW Ø 2.9x9.5
10- ACYRILIC WINDOW (001)
11- MULTIBUTON (001)
12- MULTIBUTON PCB SCREW Ø 2.9x9.5
13- REMOTE PCB
14- REMOTE PCB SCREW Ø 2.9x6.5
15- ON-OFF BUTON
16- ON-OFF BUTON SPRING
17- ON-OFF HAT
18- ON-OFF PCB
19- ON-OFF PCB HOLDER
20- AV HOLDER 1
21- AV HOLDER SCREW Ø 2.9x13
22- AV HOLDER 2
23- AV PCB
24- AV PCB SCREW Ø 2.9x6.5
25- AV HOLDER SPRING
26- CHASSIS RAIL RIGHT
27- CHASSIS RAIL LEFT
28- CHASSIS RAIL SCREW Ø 3.9x9.5
29- FRAME MAIN PCB
30- MAIN PCB
31- BACK COWER
32- BACK COWER SCREW Ø 3.9x19
33- HORN DOOR
34- DOOR LOCK
35- 32" 16/9 NOVA STYROPHOR
36- LOGO
37-
38-

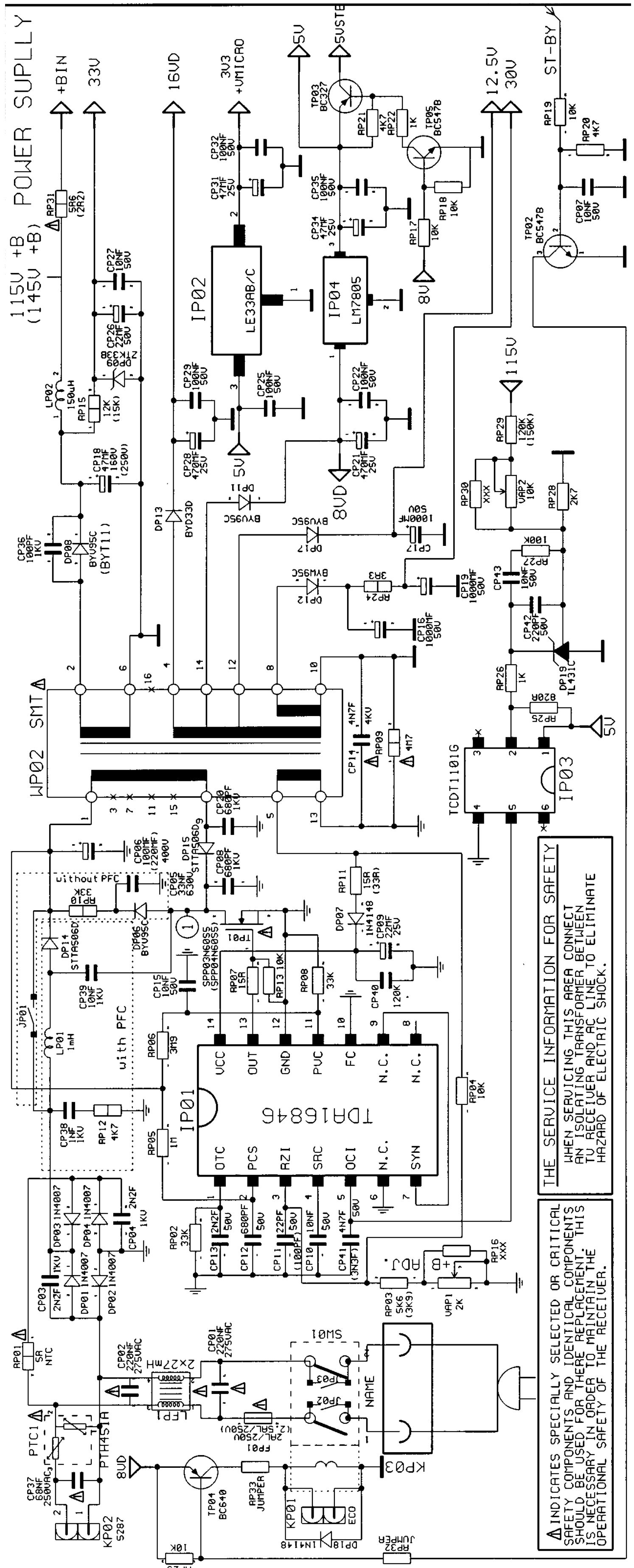
PT92 110° STEREO CHASSIS



FAULT TRACING DIAGRAM-POWER SUPPLY



POWER SUPPLY



TROUBLESHOOTING GUIDE FOR MAIN PCB

TROUBLE	CHECK POINTS
No color	CV37, CV38, XV01
Horizontal linearity	LD02, RD20, DD06
Horizontal size	+B voltage, CD18, CD20, CD27, CD08, TV06
Flue picture	RD17, RD06, RD62, R001, Focus adjust
Dark picture	Screen adjust, EHT voltage
Noise picture	TU01, AGC adjust, If adjust
Interference	TV01, TV04, TU01
No sound	IA50, IA51, IA01, DP17, DP12, RA51, X301, I302, IV01
Sound distortion	I302, IC01, L304, CA07, CA06, RA06, RA07, IA01, IA50, IA51
Memory	IC02, IV01, TC10
No video on the SCART	IV01, TE01, TE04
No audio on the SCART	I302, TV03
No picture	TD01, TD02, DD01, TD04, DD03, DD04, ID50, RD56, IV01

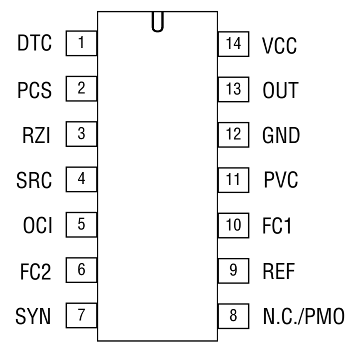
TDA16846

Controller For Switch Mode Power Supplies

The TDA16846 is suited for TV-, VCR-sets and SAT receivers. It also can be good used in PC monitors.

The TDA 16847 is identical with TDA16846 but has an additional power measurement output (pin 8) which can be used a Temporary High Power Circuit.

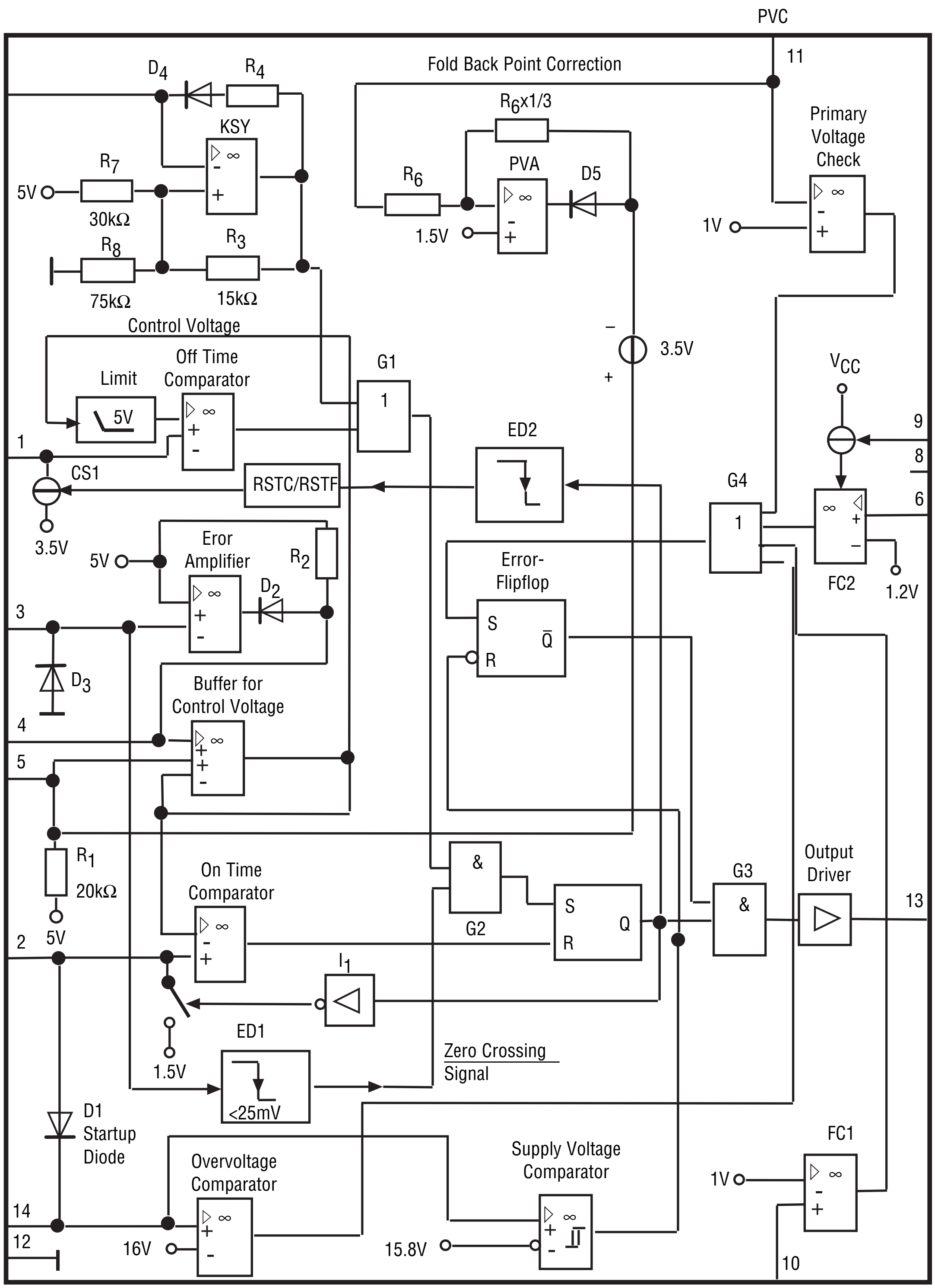
Pin Configuration (top view)



Pin Definitions and Functions

Pin	Symbol	Function
1	OTC	Off Time Circuit
2	PCS	Primary Current Simulation
3	RZI	Regulation and Zero Crossing Input
4	SRC	Soft-Start and Regulation Capacitor
5	OCI	Opto Coupler Input
6	FC2	Fault Comparator 2
7	SYN	Synchronization Input
8	N.C./PMO	Not Connected (TDA16846)
9	REF	Reference Voltage and Current
10	FC1	Fault Comparator 1
11	PVC	Primary Voltage Check
12	GND	Ground
13	OUT	Output
14	VCC	Supply Voltage

TDA16846 Block Diagrams



1) The input with the lower voltage becomes operative

ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

All voltages listed are referenced to ground (0V, Vss) except where noted.

Parameter	Symbol	Limit Values		Unit	Remarks
		Min.	Typ.		
Supply Voltage at Pin 14	V_{cc}	-0.3	17	V	-
Voltage at Pin 1, 4, 5, 6, 7, 9, 10	-	-0.3	6	V	-
Voltage at Pin 2, 8, 11	-	-0.3	17	V	-
Voltage at Pin 3	RZI		6	V	-
Current into Pin 3		-10		mA	$V_3 < - 0.3V$
Current into Pin 9	REF	-1	-	mA	-
Current into Pin 13	OUT	 -100	100	mA mA	$V_{13} > - V_{cc}$ $V_{13} < - 0V$
ESD Protection	-	-	2	kV	MIIL STD 883C methot 3015.6, 100 PF, 1500Ω
Storage Temperature	T_{stg}	-65	125	°C	-
Operating Junction Temperature	T_j	-	125	°C	-
Thermal Resistance Junction-Ambient	R_{thJA}	-	110	K/W	P-DIP-14-3
Soldering Temperature	-	-	260	°C	-
Soldering Time -	-	10	s	-	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Short Description of the Pin Functions

Pin	Functions
1	A parallel RC-circuit between this pin and ground determines the ringing suppression time and the standby-frequency.
2	A capacitor between this pin and ground and a resistor between this pin and the positive terminal of the primary elcap quantifies the max. possible output power of the SMPS.
3	This is the input of the error amplifier and the zero crossing input. The output of a voltage divider between the control winding and ground is connected to this input. If the pulses at pin 3 exceed a 5 V threshold, the control voltage at pin 4 is lowered.
4	This is the pin for the control voltage. A capacitor has to be connected between this pin and ground. The value of this capacitor determines the duration of the softstart and the speed of the control.
5	If an opto coupler for the control is used, it's output has to be connected between this pin and ground. The voltage divider at pin 3 has then to be changed, so that the pulses at pin 3 are below 5 V.
6	Fault comparator 2: If a voltage > 1.2 V is applied to this pin, the SMPS stops.
7	If fixed frequency mode is wanted, a parallel RC circuit has to be connected between this pin and ground. The RC-value determines the frequency. If synchronized mode is wanted, sync pulses have to be fed into this pin.
8	Not connected (TDA16846). / This is the power measurement output of the Temporary High Power Circuit. A capacitor and a RC-circuit has to be connected between this pin and ground.
9	Output for reference voltage (5 V). With a resistor between this pin and ground the fault comparator 2 (pin 6) is enabled.
10	Fault comparator i: If a voltage > 1 V is applied to this pin, the SMPS stops.
11	This is the input of the primary voltage check. The voltage at the anode of the primary elcap has to be fed to this pin via a voltage divider. If the voltage of this pin falls below 1 V, the SMPS is switched off. A second function of this pin is the primary voltage dependent fold back point correction (only active in free running mode).
12	Common ground.
13	Output signal. This pin has to be connected across a serial resistor with the gate of the power transistor.
14	Connection for supply voltage and startup capacitor. After startup the supply voltage is produced by the control winding of the transformer and rectified by an external diode.

TDA935X/6X/8X
TV signal processor-Teletext decoder with embedded μ-Controller

GENERAL DESCRIPTION

The various versions of the TDA935X/6X/8X series combine the functions of a n/ signal processor together with a µ-Controller and US Closed Caption decoder. Most versions have a Teletext decoder on board. The Teletext decoder has an internal RAM memory for 1 or 10 page text. The ICs are intended to be used in economy television receivers with 90° and 110° picture tubes.

The ICs have supply voltages of 8 V and 3.3 V and they are mounted in S-DIP envelope with 64 pins.

The features are given in the following feature list. The differences between the various ICs are given in the table on page 4.

FEATURES

TV-signal processor

- Multi-standard vision IF circuit with alignment-free PLL demodulator
- Internal (switchable) time-constant for the IF-AGC circuit
- A choice can be made between versions with mono intercarrier sound FM demodulator and versions with QSS IF amplifier.
- The mono intercarrier sound versions have a selective FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted.
- Source selection between 'internal' CVBS and external CVBS or Y/C signals
- Integrated chrominance trap circuit
- Integrated luminance delay line with adjustable delay time
- Asymmetrical 'delay line type' peaking in the luminance channel
- Black stretching for non-standard luminance signals
- Integrated chroma band-pass filter with switchable centre frequency
- Only one reference (12 MHz) crystal required for the CL-Controller, Teletext- and the colour decoder
- PAL/NTSC or multi-standard colour decoder with automatic search system
- Internal base-band delay line
- RGB control circuit with 'Continuous Cathode Calibration', white point and black level off set adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
- Linear RGB or YUV input with fast blanking for external RGB/YUV sources. The Text/OSD signals are internally supplied from the µ-Controller/Teletext decoder
- Contrast reduction possibility during mixed-mode of OSD and Text signals
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Horizontal and vertical geometry processing
- Horizontal and vertical zoom function for 16 : 9 applications
- Horizontal parallelogram and bow correction for large screen picture tubes

µ-CONTROLLER

- 80C51 µ-controller core standard instruction set and timing
- 1 µs machine cycle
- 32 - 128Kx8-bit late programmed ROM
- 3 - 12Kx8-bit Auxiliary RAM (shared with Display and Acquisition)
- Interrupt controller for individual enable/disable with two level priority
- Two 16-bit Timer/Counter registers
- WatchDog timer
- Auxiliary RAM page pointer
- 16-bit Data pointer
- IDLE and Power Down (PD) mode
- 14 bits PWM for Voltage Synthesis Tuning
- 8-bit A/D converter
- 4 pins which can be programmed as general I/O pin, ADC input or PWM (6-bit) output

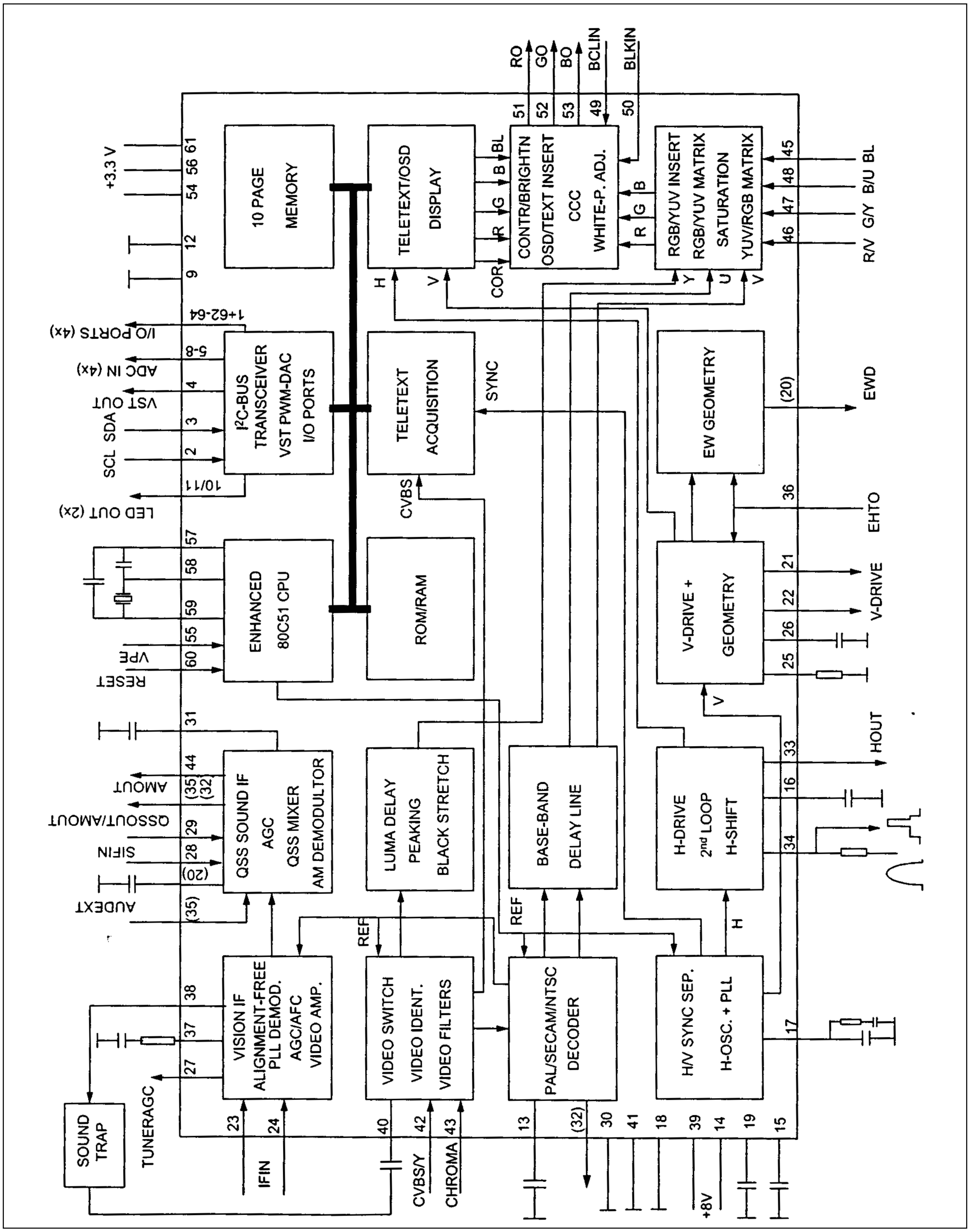
DATA CAPTURE

- Text memory for 1 or 10 pages
- In the 10 page versions inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT)
- Data Capture for US Closed Caption
- Data Capture for 525/625 line WST, VPS (PDC system A) and Wise Screen Signalling (WSS) bit decoding
- Automatic selection between 525 WST/625 WST
- Automatic selection between 625 WST/VPS on line 16 of VBI
- Real-time capture and decoding for WST Teletext in Hardware, to enable optimized µ-processor throughput
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine in Hardware for processing accented, G2 and G3 characters
- Signal quality detector for video and WST/VPS data types
- Comprehensive teletext language coverage
- Full Field and Vertical Blanking Interval (VBI) data capture of WST data

DISPLAY

- Teletext and Enhanced OSD modes
- Features of level 1.5 WST and US Close Caption
- Serial and Parallel Display Attributes
- Single/Double/Quadruple Width and Height for characters
- Scrolling of display region
- Variable flash rate controlled by software
- Enhanced display features including overlining, underlining and italics
- Soft colours using CLUT with 4096 colour palette
- Globally selectable scan lines per row (9/10/13/16) and character matrix [12x10, 12x13, 12x16 (VxH)]
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics Characters with two planes, allowing four colours per character
- 32 software redefinable On-Screen display characters
- 4 WST Character sets (GO/G2) in single device (e.g. Latin, Cyrillic, Greek, Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST Character sets and Closed Caption Character set in single device.

Block Diagram



QUICK REFERENCE DATA

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit
Supply					
V_P	supply voltage	-	8.0/3.3	-	V
I_p	supply current	-	tbf	-	mA
Input voltages					
$V_{iSIF(rms)}$	video IF amplifier sensitivity (RMS value)	-	35	-	µV
$V_{iVIF(rms)}$	QSS sound IF amplifier sensitivity (RMS value)	-	60	-	µV
$V_{iAUDIO(rms)}$	external audio input (RMS value)	-	500	-	mV
$V_{iCVBS(p-p)}$	external CVBS/Y input (peak-to-peak value)	-	1.0	-	V
$V_{iCHORAMA(p-p)}$	external chroma input voltage (burst amplitude) (peak-to-peak value)	-	0.3	-	V
$V_{iRGB(p-p)}$	RGB inputs (peak-to-peak value)	-	0.7	-	V
$V_{iYIN(p-p)}$	luminance input signal (peak-to-peak value)	-	1.4	-	V
$V_{iUVIN(p-p)}$	U/V input signal (peak-to-peak value)	-	1.33/1.05	-	V
Output signals					
$V_{o(IFVO(p-p)}$	demodulated CVBS output (peak-to-peak value)	-	2.5	-	V
$V_{o(QSSO)(rms)}$	sound IF intercarrier output in QSS versions (RMS value)	-	100	-	mV
$V_{o(AMOUT)(rms)}$	demodulated AM sound output in QSS versions (RMS value)	-	500	-	mV
$I_{o(AGCOUT)}$	tuner AGC output current range	0	-	5	mV
$V_{oRGB(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	-	2.0	-	V
$I_{o\ HOUT}$	horizontal output current	10	-	-	mA
$I_{o\ VERT}$	vertical output current (peak-to-peak value)	1	-	-	mA
$I_{o\ EWD}$	EW drive output current	1.2	-	-	mA

PINNING

SYMBOL	PIN	DESCRIPTION
P1.3TT1	1	port 1.3 or Counter/Timer 1 input
P1.6/SCL	2	port 1.6 or I²C-bus clock line
P1.7/SDA	3	port 1.7 or I²C-bus data line
P2. O/TPWM	4	port 2.0 or Tuning PWM output
P3.0/ADC0	5	port 3.0 or ADC0 input
P3.1/ADCI	6	port 3.1 or ADC1 input
P3.2/ADC2	7	port 3.2 or ADC2 input
P3.3/ADC3	8	port 3.3 or ADC3 input
VSSC/P	9	digital ground for µ-Controller core and periphery
P0.5	10	port 0.5 (8 mA current sinking capability for direct drive of LEDs)
P0.6	11	port 0.6 (8 mA current sinking capability for direct drive of LEDs)
VSSA	12	analog ground of Teletext decoder and digital ground of TV- processor
SECPLL	13	SECAM PLL decoupling
VP2	14	2nd supply voltage TV-processor (+8V)
DECDIG	15	decoupling digital supply of TV-processor
PH2LF	16	phase-2 filter
PH1LF	17	phase-1 filter
GND3	18	ground 3 for TV-processor
DECBG	19	bandgap decoupling
AVL/EWD(1)	20	Automatic Volume Levelling /East-West drive output
VDRB	21	vertical drive B output
VDRA	22	vertical drive A output
IFIN1	23	IF input 1
IFIN2	24	IF input 2
IREF	25	reference current input
VSC	26	vertical sawtooth capacitor
TUNERAGC	27	tuner AGC output
AUDEEM/SIFIN1(1)	28	audio deemphasis or SIF input 1
DECSDEM/SIFIN2(1)	29	decoupling sound demodulator or SIF input 2
GND2	30	ground 2 for TV-processor
SNDPLL/SIFAGC(1)	31	narrow band PLL filter / AGC sound IF
AVL/REF0/AMOUT(1)	32	Automatic Volume Levelling / subcarrier reference output/AM output (non controlled)
HOUT	33	horizontal output
FBISO	34	flyback input/sandcastle output
AUDEXT/ QSSO/AMOUT(1)	35	external audio input/QSS intercarrier out /AM audio output (non controlled)
EHTO	36	EHT/overvoltage protection input
PLLIF	37	IF-PLL loop filter
IFVO/SVO	38	IF video output / selected CVBS output
VP1	39	main supply voltage TV-processor (+8 V)
CVBSINT	40	internal CVBS input

PINNING

SYMBOL	PIN	DESCRIPTION
GND1	41	ground 1 for TV-processor
CVBS/Y	42	external CVBS/Y input
CHROMA	43	chrominance input (SVHS)
AUDOUT / AMOUT [(1)]	44	audio output / AM audio output (volume controlled)
INSSW2	45	2nd RGB /YUV insertion input
R2/VIN	46	2nd R input / V (R-Y) input
G2 YIN	47	2nd G input Y input
B2 UIN	48	2nd B input / U (B-Y) input
BCLIN	49	beam current limiter input/V-guard input
BLKIN	50	black current input
RO	51	Red output
GO	52	Green output
BO	53	Blue output
VDDA	54	analog supply of Teletext decoder and digital supply of TV-processor (3.3 V)
VPE	55	OTP Programming Voltage
VDDC	56	digital supply to core (3.3V)
OSCGND	57	oscillator ground supply
XTALIN	58	crystal oscillator input
XTALOUT	59	crystal oscillator output
RESET	60	reset
VDDP	61	digital supply to periphery (+3.3 V)
P1.0/INT1	62	port 1.0 or external interrupt 1 input
P1.1/T0	63	port 1.1 or Counter/Timer 0 input
P1.2/INT0	64	port 1.2 or external interrupt 0 input

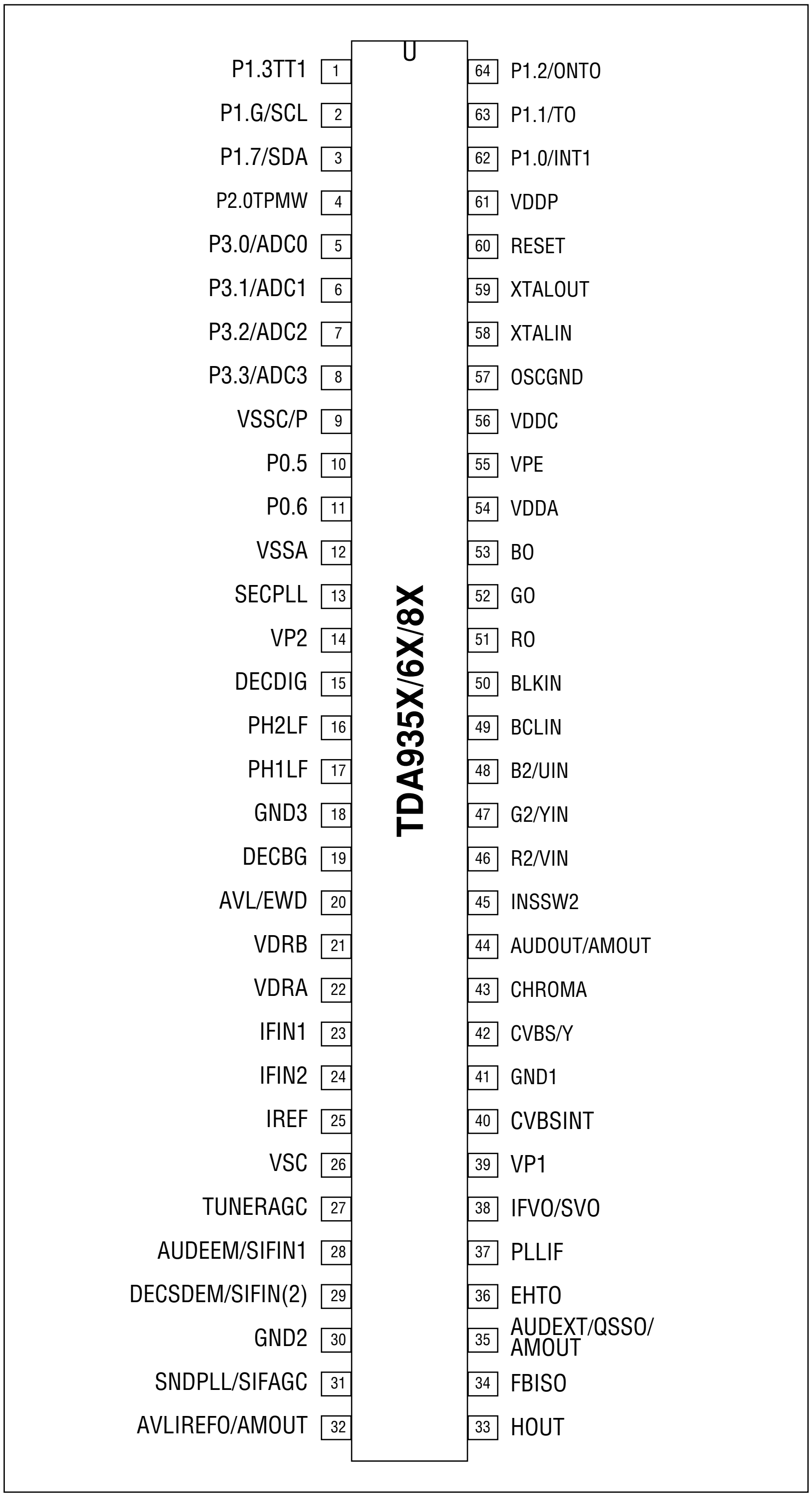
Note

1. The function of pin 20, 28, 29, 31, 32, 35 and 44 is dependent on the IC version (mono irtercarrier FM demodulator / QSS IF amplifier and East-West output or not) and on some software control bits. The valid combinations are given in table 1.

Table 1 Pin functions for various versions

IC version	FM-PLL version			QSS version					
East-West Y/N	N	Y		N			Y		
CMB1/CMB0 bits	-	00	01/10/11	00	01/10/11		00	01/10/11	
AM bit	-	-	-	-	0	1	-	0	1
Pin 20	AVL	EWD		AVL			EWD		
Pin 28	AUDEEM			SIFIN1					
Pin 29	DECSDEM			SIFIN2					
Pin 31	SNDPLL			SIFAGC					
Pin 32	REFO	AVL	REFO	AMOUT	REFO		AMOUT	REFO	
Pin 35	AUDEXT			AUDEX	QSSO	AMOUT	AUDEXT	QSSO	AMOUT
Pin 44	AUDOUT			controlled AM out					

Pin configuration (SDIP 64)



TDA9875A
Digital TV sound processor (DTVSP)

FEATURES

1.1 Demodulator and decoder section

- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF AGC with 24 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- DQPSK demodulation for different standards, simultaneously with 1-channel FM demodulation
- NICAM decoding (B/G, I and L standard)
- Two-carrier multistandard FM demodulation (B/G, D/K and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound
- Optional AM demodulation for system L, simultaneously with NICAM
- Programmable identification (B/G, D/K and M standard) and different identification times.

1.2 DSP section

- Digital crossbar switch for all digital signal sources and destinations
- Control of volume, balance, contour, bass, treble, pseudo stereo, spatial, bass boost and soft-mute
- Plop-free volume control
- Automatic Volume Level (AVL) control
- Adaptive de-emphasis for satellite
- Programmable beeper
- Monitor selection for FM/AM DC values and signals, with peak detection option
- I^2S-bus interface for a feature extension (e.g. Dolby surround) with matrix, level adjust and mute.

1.3 Analog audio section

- Analog crossbar switch with inputs for mono and stereo (also applicable as SCART 3 input), SCART 1 input/output, SCART 2 input/output and line output
- User defined full-level/-3 dB scaling for SCART outputs
- Output selection of mono, stereo, dual A/B, dual A or dual B
- 20 kHz bandwidth for SCART-to-SCART copies
- Standby mode with functionality for SCART copies
- Dual audio digital-to-analog converter from DSP to analog crossbar switch, bandwidth 15 kHz
- Dual audio ADC from analog inputs to DSP
- Two dual audio Digital-to-Analog Converters (DACs) for loudspeaker (Main) and headphone (Auxiliary) outputs; also applicable for L, R, C and S in the Dolby Pro Logic mode with feature extension.

2 GENERAL DESCRIPTION

The TDA9875A is a single-chip Digital TV Sound Processor (DTVSP) for analog and digital multi-channel sound systems in TV sets and satellite receivers.

2.1 Supported standards

The multistandard/multi-stereo capability of the TDA9875A is mainly of interest in Europe, but also in Hong Kong/Peoples Republic of China and South East Asia. This includes B/G, D/K, 1, M and L standard. In other application areas there exists only subsets of those standard combinations otherwise only single standards are transmitted.

M standard is transmitted in Europe by the American Forces Network (AFN) with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

The AM sound of L/L standard is normally demodulated in the 1st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9875A. A second possibility is to use the internal AM demodulator stage, however this gives limited performance.

Korea has a stereo sound system similar to Europe and is supported by the TDA9875A. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards and sound systems and their key parameters is given in Table 1.

The analog multi-channel sound systems (A2, A2+ and A2*) are sometimes also named 2CS (2 carrier systems).

2.1.1 ANALOG 2-CARRIER SYSTEMS

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz) NOM./MAX./OVER	MODULATION		BANDWIDTH DE-EMPHASIS (kHz/µs)
				SC1	SC2	
M	mono	4.5	15/25/50	mono	-	15/75
M	A2+	4.5/4.724	15/25/50	1/2 (L + R)	1/2 (L - R)	15/75 (Korea)
B/G	A2	5.5/5.742	27/50/80	1/2 (L + R)	R	15/50
I	mono	6.5/6.742	27/50/80	mono	-	15/50
D/K	A2	6.5/6.742	27/50/80	1/2 (L + R)	R	15/50
D/K	A2*	6.5/6.258	27/50/80	1/2 (L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2/A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 x line frequency	55.0699 kHz = 3.5 x line frequency
Stereo identification frequency	117.5 Hz = line frequency / 133	149.9 Hz = line frequency / 105
Dual identification frequency	274.1Hz = line frequency / 57	276.0 Hz = line frequency / 57
AM modulation depth	50%	50%

2.1.2 2-CARRIER SYSTEMS WITH NICAM

Table 3 NICAM

STANDARD	SC1				SC2 (MHz) NICAM	DE-EMPHASIS	ROLL-OFF (%)	NICAM CODING
	FREQUENCY (MHz)	TYPE	MODULATION					
			INDEX (%) NOM./MAX.	DEVIATION (kHz) NOM./MAX.				
B/G	5.5	FM	-	27/50	5.85	J17	40	note 1
I	6.0	FM	-	27/50	6.552	J17	100	note 1
D/K	6.5	FM	-	27/50	5.85	J17	40	note 2
L	6.5	AM	54/100	-	5.85	J17	40	note 1

Notes

1. See “EBU specification” or equivalent specification.
2. Not yet defined

2.1.3 SATELLITE SYSTEMS

An important for satellite TV reception is the ‘Astra specification”. The TDA9875A is suited for the reception of Astra and other satellite signals.

Table 4 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH DE-EMPHASIS (kHz/μs)
main	6.50[(1)]	0.26	85	mono	15/50[(1)]
sub	7.02/7.20	0.15	50	m/st/d[(2)]	15/adaptive[(3)]
sub	7.38/7.56	0.15	50	m/st/d[(2)]	15/adaptive[(3)]
sub	7.74/7.92	0.15	50	m/st/d[(2)]	15/adaptive[(3)]
sub	8.10/8.28	0.15	50	m/st/d[(2)]	15/adaptive[(3)]

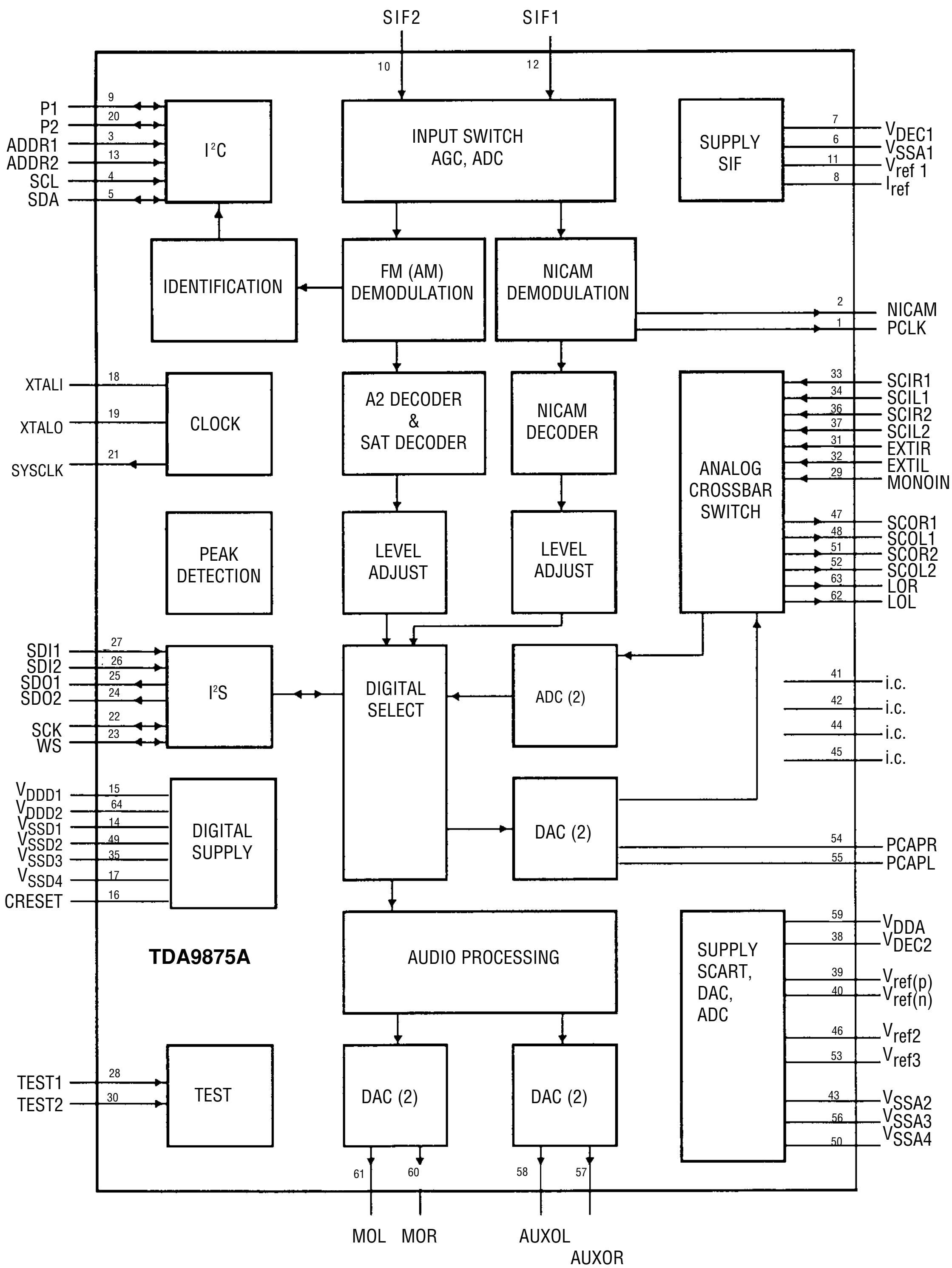
Notes

1. For other satellite systems, frequencies of, for example, 5.80, 6.60 or 6.65 MHz can also be received. A de-emphasis of 60 μs, or in accordance with J17, is available.
2. m/st/d = mono or stereo or dual language sound.
3. Adaptive de-emphasis = compatible to transmitter specification.

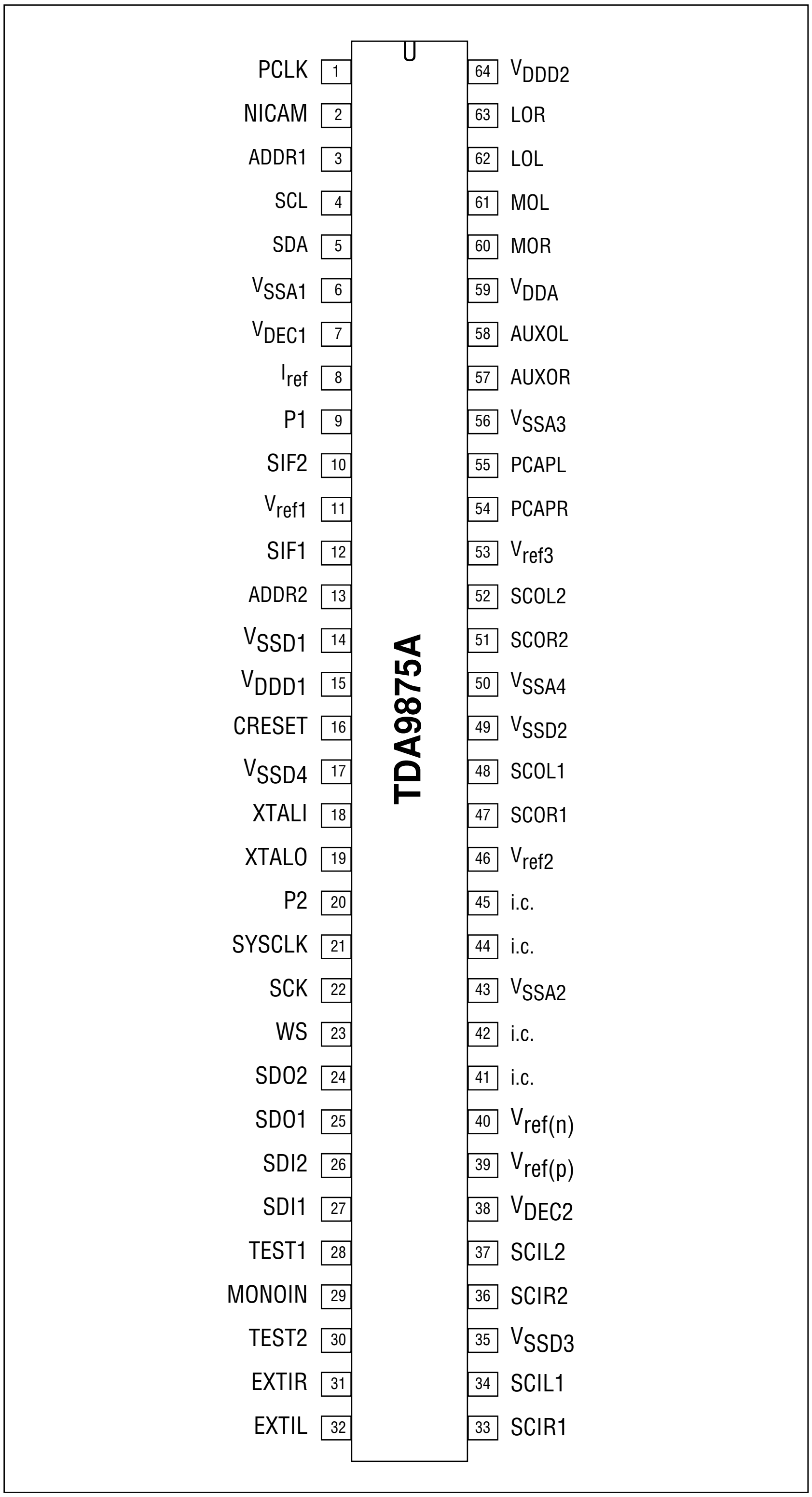
3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9875A	SDIP64	plastic shrink dual-in-line package; 64 leads (750 mil)	SOT274-1

Block Diagram



Pin configuration



SYMBOL	PIN	I/O	DESCRIPTION
PCLK	1	O	NICAM clock output at 728 Khz
NICAM	2	O	serial NICAM data output at 728 kHz
ADDR1	3	I	first I^2C-bus slave address modifier
SCL	4	I	I^2C-bus clock
SDA	5	I/O	I^2C-bus data
V_{SSA1}	6	supply	supply ground 1; analog front-end circuitry
V_{DEC1}	7	-	positive power supply voltage 1 decoupling; analog front-end circuitry
I_{ref}	8	-	resistor for reference current generator; analog front-end circuitry
P1	9	I/O	first general purpose I/O pin
SIF2	10	-	sound IF input 2
V_{ref1}	11	-	reference voltage; analog front-end circuitry
SIF1	12	I	sound IF input 1
ADDR2	13	I	second I^2C-bus slave address modifier
V_{SSD1}	14	supply	supply ground 1; digital circuitry
V_{DDD1}	15	supply	digital supply voltage 1; digital circuitry
CRESET	16	-	capacitor for power-on reset
V_{SSD4}	17	supply	supply ground 4; digital circuitry
XTALI	18	I	crystal oscillator input
XTALO	19	O	crystal oscillator output
P2	20	I/O	second general purpose I/O pin
SYSCLK	21	O	system clock output
SCK	22	I/O	I^2C-bus clock
WS	23	I/O	I^2C-bus word select
SDO2	24	O	I^2C-bus data output 2
SDO1	25	O	I^2C-bus data output 1
SDI2	26	I	I^2C-bus data input 2
SDI1	27	I	I^2C-bus data input 1
TEST1	28	I	first test pin; connected to V_{SSD1} for normal operation
MONOIN	29	I	audio mono input
TEST2	30	I	second test pin; connected to V_{SSD1} for normal operation
EXTIR	31	I	external audio input right channel
EXTIL	32	I	external audio input left channel
SCIR1	33	I	SCART 1 input right channel
SCIL1	34	I	SCART 1 input left channel
V_{SSD3}	35	supply	supply ground 3; digital circuitry
SCIR2	36	I	SCART 2 input right channel
SCIL2	37	I	SCART 2 input left channel
V_{DEC2}	38	-	positive power supply voltage 2 decoupling; audio analog to digital converter circuitry

SYMBOL	PIN	I/O	DESCRIPTION
$V_{ref(p)}$	39	-	positive reference voltage; audio analog to digital converter circuitry
$PCLKV_{ref(n)}$	40	-	reference voltage ground; audio analog-to-digital converter circuitry
i.c.	41	-	internally connected; note 1
i.c.	42	-	internally connected; note 2
V_{SSA2}	43	supply	supply ground; audio analog-to-digital converter circuitry
i.c.	44	-	internally connected; note 2
i.c.	45	-	internally connected; note 1
V_{ref2}	46	-	reference voltage; audio analog-to-digital converter circuitry
SCOR1	47	O	SCART 1 output right channel
SCOL1	48	O	SCART 1 output left channel
V_{SSD2}	49	supply	supply ground 2; digital circuitry
V_{SSA4}	50	supply	supply ground 4; audio operational amplifier circuitry
SCOR2	51	O	SCART 2 output right channel
SCOL2	52	O	SCART 2 output left channel
V_{ref3}	53	-	reference voltage; audio digital to analog converter and operational amplifier circuitry
PCAPR	54	-	post filter capacitor pin right channel, audio digital-to-analog converter
PCAPL	55	-	post filter capacitor pin left channel, audio digital-to-analog converter
V_{SSA3}	56	supply	supply ground 3; audio analog-to-digital converter circuitry
AUXOR	57	O	headphone (auxiliary) output right channel
AUXOL	58	O	headphone (auxiliary) output left channel
V_{DDA}	59	O	positive analog power supply voltage; analog circuitry
MOR	60	O	loudspeaker (Main) output right channel
MOL	61	supply	loudspeaker (Main) output left channel
LOL	62	O	line output left channel
LOR	63	O	line output right channel
V_{DDD2}	64	supply	digital supply voltage 2; digital circuitry

Notes

1. Test pin, CMOS level input, pull-up resistor, can be connected to V_{SS}.
2. Test pin, CMOS 3-state stage, can be connected to V_{SS}.

TDA9870A

Digital TV sound processor (DTVSP)

FEATURES

1.1 Demodulator and decoder section

- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF AGC with 24 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- Two-carrier multistandard FM demodulation (B/G, D/K and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound
- Programmable identification (B/G, D/K and M standard) and different identification times.

1.2 DSP section

- Digital crossbar switch for all digital signal sources and destinations
- Control of volume, balance, contour, bass, treble, pseudo stereo, spatial, bass boost and soft-mute
- Plop-free volume control
- Automatic Volume Level (AVL) control
- Adaptive de-emphasis for satellite
- Programmable beeper
- Monitor selection for FM/AM DC values and signals, with peak detection option
- I^2S-bus interface for a feature extension (e.g. Dolby surround) with matrix, level adjust and mute.

1.3 Analog audio section

- Analog crossbar switch with inputs for mono and stereo (also applicable as SCART 3 input), SCART 1 input/output, SCART 2 input/output and line output
- User defined full-level/-3 dB scaling for SCART outputs
- Output selection of mono, stereo, dual A/B, dual A or dual B
- 20 kHz bandwidth for SCART-to-SCART copies
- Standby mode with functionality for SCART copies
- Dual audio digital-to-analog converter from DSP to analog crossbar switch, bandwidth 15 kHz
- Dual audio ADC from analog inputs to DSP
- Two dual audio Digital-to-Analog Converters (DACs) for loudspeaker (Main) and headphone (Auxiliary) outputs; also applicable for L, R, C and S in the Dolby Pro Logic mode with feature extension.

2 GENERAL DESCRIPTION

The TDA9870A is a single-chip Digital TV Sound Processor (DTVSP) for analog multi-channel sound systems in TV sets and satellite receivers.

2.1 Supported standards

The multistandard/multi-stereo capability of the TDA9870A is mainly of interest in Europe, but also in Hong Kong/Peoples Republic of China and South East Asia.

This includes B/G, D/K, I, M and L standard. In other application areas there exists only subsets of those standard combinations otherwise only single standards are transmitted.

M standard is transmitted in Europe by the American Forces Network (AFN) with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

Korea has a stereo sound system similar to Europe and is supported by the TDA9870A. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards and sound systems and their key parameters is given in.(Table 1).

The analog multi-channel sound systems (A2, A2+ and AP) are sometimes also named 2CS (2 carrier systems).

2.1.1 ANALOG 2-CARRIER SYSTEMS

Table 1 Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHz)	FM DEVIATION (kHz) NOM./MAX./OVER	MODULATION		BANDWIDTH DE-EMPHASIS (kHz/µs)
				SC1	SC2	
M	mono	4.5	15/25/50	mono	-	15/75
M	A2+	4.5/4.724	15/25/50	1/2 (L + R)	1/2 (L - R)	15/75 (Korea)
B/G	A2	5.5/5.742	27/50/80	1/2 (L + R)	R	15/50
I	mono	6.0	27/50/80	mono	-	15/50
D/K	A2	6.5/6.742	27/50/80	1/2 (L + R)	R	15/50
D/K	A2*	6.5/6.258	27/50/80	1/2 (L + R)	R	15/50

Table 2 Identification for A2 systems

PARAMETER	A2/A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 x line frequency	55.0699 kHz = 3.5 x line frequency
Stereo identification frequency	117.5 Hz = $\frac{\text{line frequency}}{133}$	149.9 Hz = $\frac{\text{line frequency}}{105}$
Dual identification frequency	274.1Hz = $\frac{\text{line frequency}}{57}$	276.0 Hz = $\frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2.1.2 SATELLITE SYSTEMS

An important for satellite TV reception is the ‘Astra specification”. The TDA9875A is suited for the reception of Astra and other satellite signals.

Table 3 FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHz)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH DE-EMPHASIS (kHz/µs)
main	6.50(1)	0.26	85	mono	15/50(1)
sub	7.02/7.20	0.15	50	m/st/d(2)	15/adaptive(3)
sub	7.38/7.56	0.15	50	m/st/d(2)	15/adaptive(3)
sub	7.74/7.92	0.15	50	m/st/d(2)	15/adaptive(3)
sub	8.10/8.28	0.15	50	m/st/d(2)	15/adaptive(3)

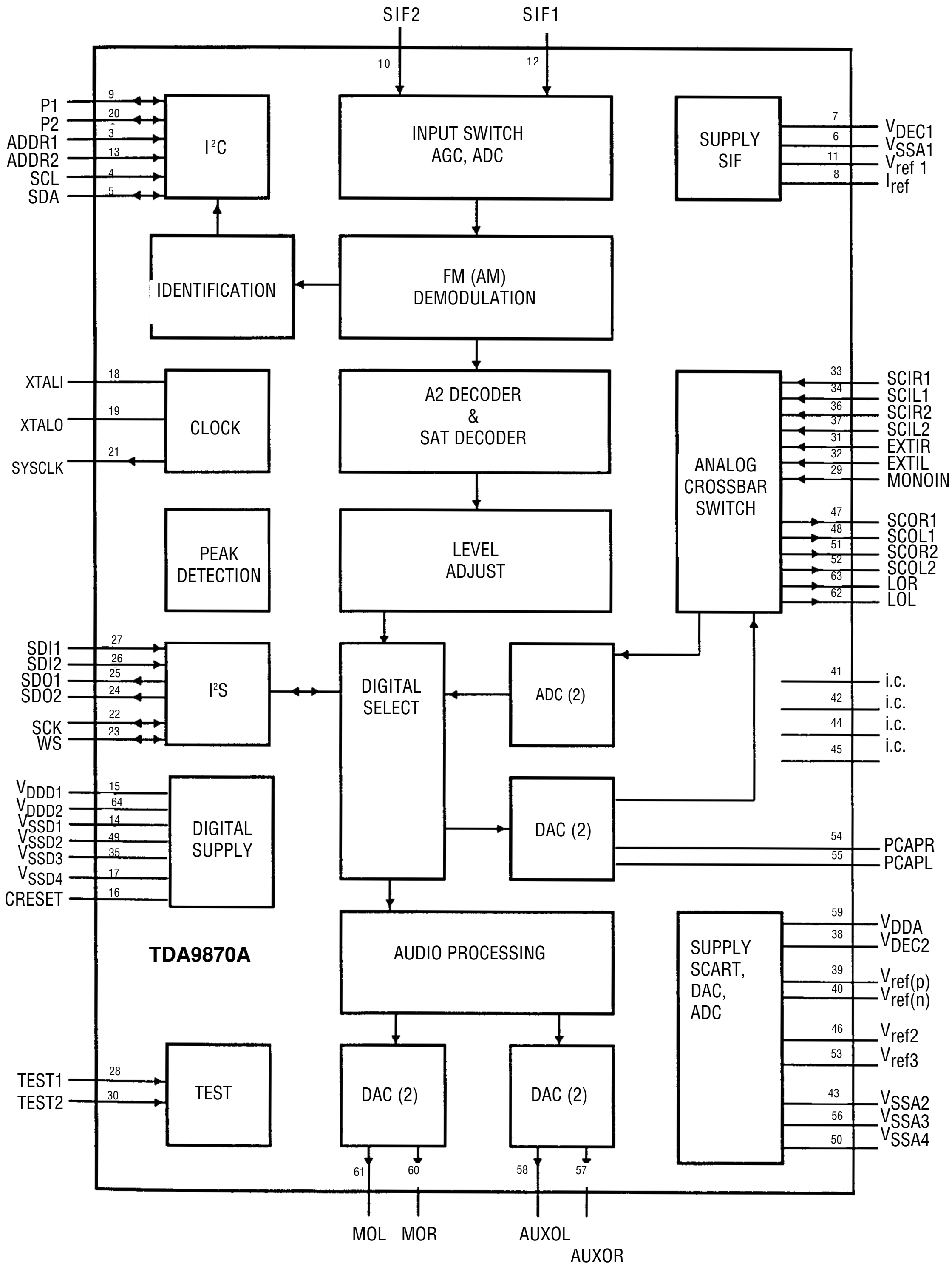
Notes

1. For other satellite systems, frequencies of, for example, 5.80, 6.60 or 6.65 MHz can also be received. A de-emphasis of 60 µs, or in accordance with J17, is available.
2. m/st/d = mono or stereo or dual language sound.
3. Adaptive de-emphasis = compatible to transmitter specification.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9875A	SDIP64	plastic shrink dual-in-line package; 64 leads (750 mil)	SOT274-1

Block Diagram



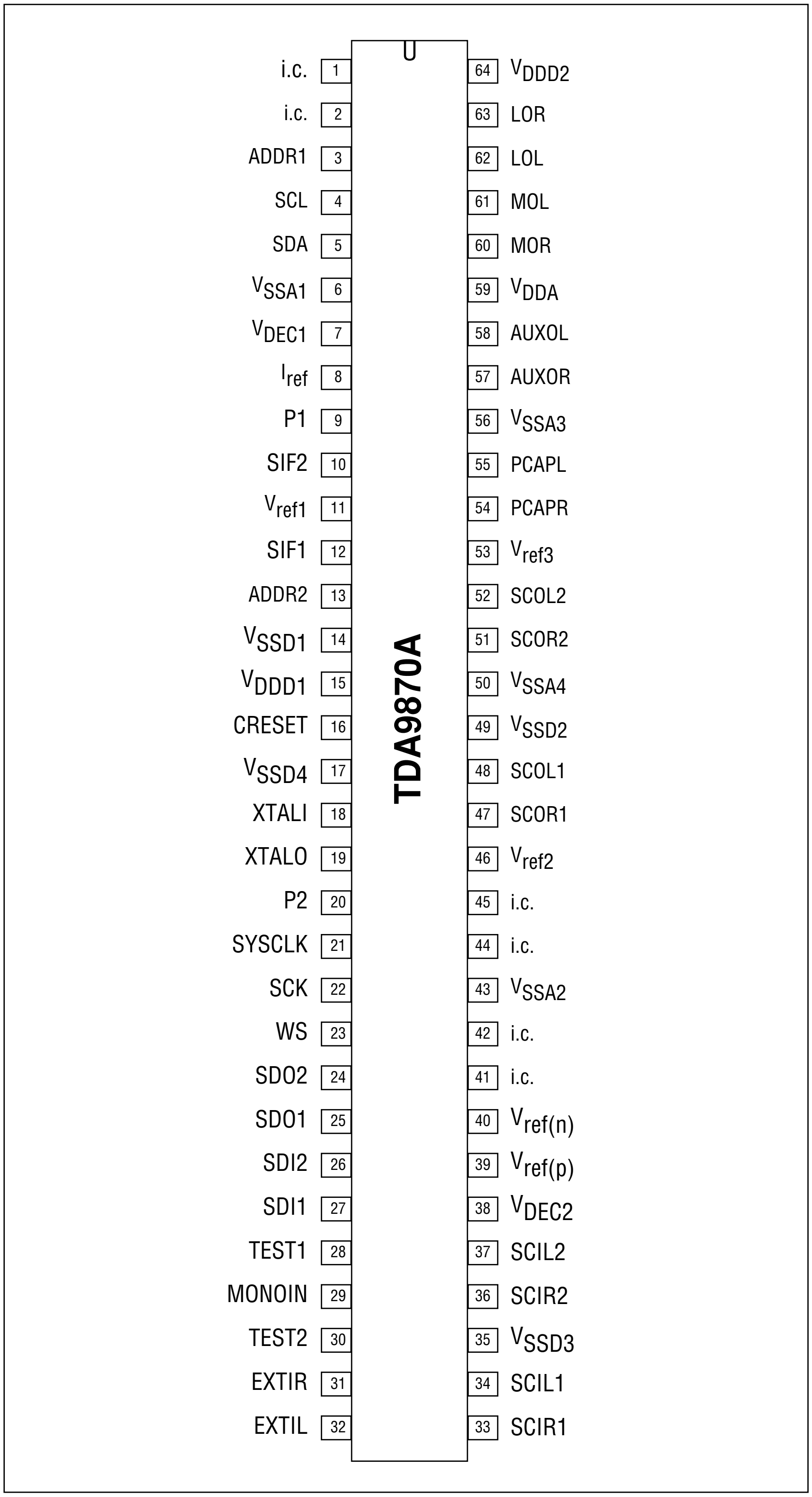
SYMBOL	PIN	I/O	DESCRIPTION
i.c.	1	-	internal connected; note 1
i.c.	2	-	internal connected; note 1
ADDR1	3	I	first I^2C-bus slave address modifier
SCL	4	I	I^2C-bus clock
SDA	5	I/O	I^2C-bus data
V_{SSA1}	6	supply	supply ground 1; analog front-end circuitry
V_{DEC1}	7	-	positive power supply voltage 1 decoupling; analog front-end circuitry
I_{ref}	8	-	resistor for reference current generator; analog front-end circuitry
P1	9	I/O	first general purpose I/O pin
SIF2	10	-	sound IF input 2
V_{ref1}	11	-	reference voltage; analog front-end circuitry
SIF1	12	I	sound IF input 1
ADDR2	13	I	second I^2C-bus slave address modifier
V_{SSD1}	14	supply	supply ground 1; digital circuitry
V_{DDD1}	15	supply	digital supply voltage 1; digital circuitry
CRESET	16	-	capacitor for power-on reset
V_{SSD4}	17	supply	supply ground 4; digital circuitry
XTALI	18	I	crystal oscillator input
XTALO	19	O	crystal oscillator output
P2	20	I/O	second general purpose I/O pin
SYSCLK	21	O	system clock output
SCK	22	I/O	I^2C-bus clock
WS	23	I/O	I^2C-bus word select
SDO2	24	O	I^2C-bus data output 2
SDO1	25	O	I^2C-bus data output 1
SDI2	26	I	I^2C-bus data input 2
SDI1	27	I	I^2C-bus data input 1
TEST1	28	I	first test pin; connected to V_{SSD1} for normal operation
MONOIN	29	I	audio mono input
TEST2	30	I	second test pin; connected to V_{SSD1} for normal operation
EXTIR	31	I	external audio input right channel
EXTIL	32	I	external audio input left channel
SCIR1	33	I	SCART 1 input right channel
SCIL1	34	I	SCART 1 input left channel
V_{SSD3}	35	supply	supply ground 3; digital circuitry
SCIR2	36	I	SCART 2 input right channel
SCIL2	37	I	SCART 2 input left channel
V_{DEC2}	38	-	positive power supply voltage 2 decoupling; audio analog to digital converter circuitry

SYMBOL	PIN	I/O	DESCRIPTION
$V_{ref(p)}$	39	-	positive reference voltage; audio analog to digital converter circuitry
$V_{ref(n)}$	40	-	reference voltage ground; audio analog-to-digital converter circuitry
i.c.	41	-	internally connected; note 2
i.c.	42	-	internally connected; note 3
V_{SSA2}	43	supply	supply ground; audio analog-to-digital converter circuitry
i.c.	44	-	internally connected; note 3
i.c.	45	-	internally connected; note 2
V_{ref2}	46	-	reference voltage; audio analog-to-digital converter circuitry
SCOR1	47	O	SCART 1 output right channel
SCOL1	48	O	SCART 1 output left channel
V_{SSD2}	49	supply	supply ground 2; digital circuitry
V_{SSA4}	50	supply	supply ground 4; audio operational amplifier circuitry
SCOR2	51	O	SCART 2 output right channel
SCOL2	52	O	SCART 2 output left channel
V_{ref3}	53	-	reference voltage; audio digital to analog converter and operational amplifier circuitry
PCAPR	54	-	post filter capacitor pin right channel, audio digital-to-analog converter
PCAPL	55	-	post filter capacitor pin left channel, audio digital-to-analog converter
V_{SSA3}	56	supply	supply ground 3; audio analog-to-digital converter circuitry
AUXOR	57	O	headphone (auxiliary) output right channel
AUXOL	58	O	headphone (auxiliary) output left channel
V_{DDA}	59	supply	positive analog power supply voltage; analog circuitry
MOR	60	O	loudspeaker (Main) output right channel
MOL	61	O	loudspeaker (Main) output left channel
LOL	62	O	line output left channel
LOR	63	O	line output right channel
V_{DDD2}	64	supply	digital supply voltage 2; digital circuitry

Notes

1. Test pin, CMOS 3-state stage, pull-up resistor, can be connected to V_{SS}.
2. Test pin, CMOS level input, pull-up resistor, can be connected to V_{SS}.
3. Test pin, CMOS 3-state stage, can be connected to V_{SS}.

Pin configuration



FUNCTIONAL DESCRIPTION

Description of the demodulator and decodersection

6.1.1 SIF INPUT

Two input pins are provided, SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. For higher SIF signal levels the SIF input can be attenuated with an internal switchable -10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

6.1.2 AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis The AGC has a fast attack behaviour to prevent ADC overloads and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen (see table 14; subaddress 0).
The AGC can be controlled via the I^2C-bus. Details can be found in the I^2C-bus register definitions (see Chapter 10).

6.1.3 MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency.
Access to the mixer control word registers is via the I^2C-bus.

6.1.4 FM AND AM DEMODULATION

An FM or AM input signal is fed via a band-limiting filter to a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for encoded satellite programs. A stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

6.1.5 FM AND AM DEMODULATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot signal and narrow-band detection of the identification frequencies. The result is available via the I^2C-bus interface. A selection can be made via the I^2C-bus for B/G, D/K and M standard and for three different modes that represent different trade-offs between speed and reliability of identification.

6.1.6 CRYSTAL OSCILLATOR

The crystal oscillator (XO) is illustrated in Fig.8 (see Chapter 12). The circuitry of the XO is fully integrated, only the external 24.576 MHz crystal is needed.

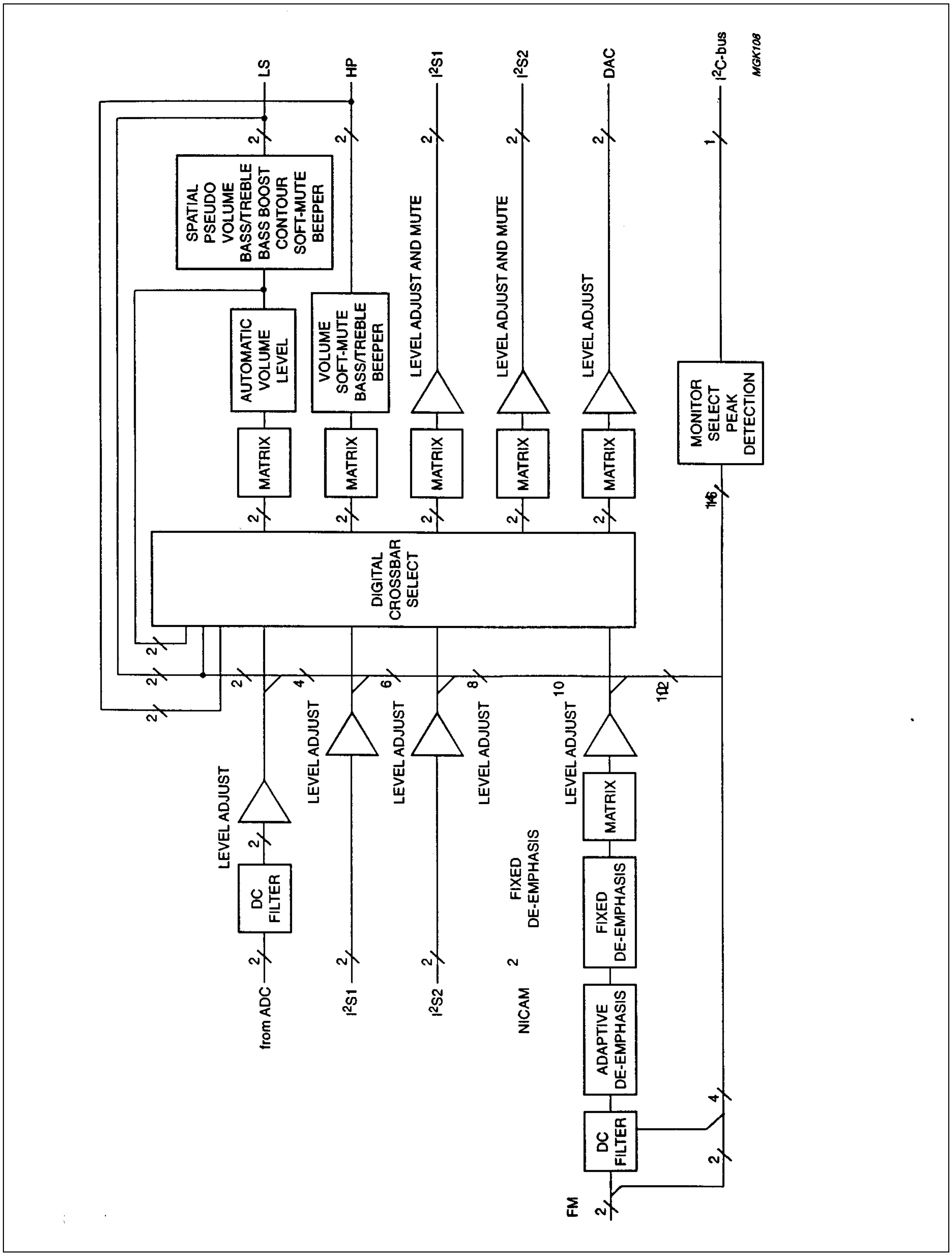
6.1.7 TEST PINS

Both test pins are active HIGH, in normal operation of the device they are wired to V_{SSD1}. Test functions are fo manufacturing tests only and are not available to customers. Without external circuitry these pads are pulled down to LOW level with internal resistors.

6.1.8 POWER-ON RESET FLIP-FLOP

The power-on reset flip-flop monitors the internal power supply for the digital part of the device. If the supply has temporary been lower than the specified lower limit, the power-on reset bit FOR, transmitter register subaddress O (see Section 10.4.1), will be set to HIGH. The CLRPOR bit, slave register subaddress 1 (see Section 10.3.2), resets the power-on reset flip-flop to LOW.

Description of the DSP



6.2.1 LEVEL SCALING

All input channels to the digital crossbar switch (except for the loudspeaker feedback path) are equipped with a level adjust facility to change the signal level in a range of ±15 dB. It is recommended to scale all input channels to be 15 dB below full scale (-15 dB full scale) under nominal conditions.

6.2.2 FM (AM) PATH

A high-pass filter suppresses DC offsets from the FM demodulator, due to carrier frequency offsets, and supplies the monitor/peak function with DC values and an unfiltered signal, e.g. for the purpose of carrier detection.

The de-emphasis function offers fixed settings for the supported standards (50 µs, 60 µs and 75 µs). An adaptive de-emphasis is available for Wegener-Panda 1 encoded programs.

A matrix performs the dematrixing of the A2 stereo, dual and mono signals.

6.2.3 MONITOR

This function provides data words from a number of locations of the signal processing paths to the I^2C-bus interface (2 data bytes). Signal sources include the FM demodulator outputs, most inputs to the digital crossbar switch and the outputs of the ADC. Source selection and data read-out is performed via the I^2C-bus.

Optionally, the peak value can be measured instead of simply taking samples. The internally stored peak value is reset to zero when the data is read via the I^2C-bus. The monitor function may be used, for example, for signal level measurements or carrier detection.

6.2.4 LOUDSPEAKER (MAIN) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel 1, channel 2 and spatial effects.

There are fixed coefficient sets for spatial settings of 30%, 40% and 52%.

The Automatic Volume Level (AVL) function provides a constant output level of -23 dB full scale for input levels between 0 and -29 dB full scale. There are some fixed decay time constants to choose from, i.e. 2, 4 and 8 s.

Pseudo stereo is based on a phase shift in one channel via a 2nd-order all-pass filter. There are fixed coefficient sets to provide 90 degrees phase shift at frequencies of 150, 200 and 300 Hz.

Volume is controlled individually for each channel ranging from +24 to -83 dB with 1 dB resolution. There is also a mute position. For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^2C-bus data byte for volume control is identical to the volume setting in dBs (e.g. the 12C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings. Contour is adjustable between 0 and +18 dB with 1 dB resolution. This function is linked to the volume setting by means of microcontroller software.

Bass is adjustable between +15 and -12 dB with 1 dB resolution and treble is adjustable between +12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^2C-bus data byte for contour, bass or treble is identical to the new contour, bass or treble setting in dBs (e.g. the I^2C-bus data byte +8 sets the new value to +8 dB).

Extra bass boost is provided up to 20 dB with 2 dB resolution. The implemented coefficient set serves merely as an example on how to use this filter.

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I^2C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full scale between 0 and -93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft mute is completed. A smooth fading is achieved by a cosine masking.

6.2.5 HEADPHONE (AUXILIARY) CHANNEL

The matrix provides the following functions; forced mono, stereo, channel swap, channel 1 and channel 2 (or C and S in Dolby Surround Pro Logic mode).

Volume is controlled individually for each channel in a range from +24 to -83 dB with 1 dB resolution. There is also a mute position.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^2C-bus data byte for volume control is identical to the volume setting in dB (e.g. the 12C-bus data byte +10 sets the new volume value to +10 dB).

Balance can be realized by independent control of the left and right channel volume settings.

Bass is adjustable between +15 and -12 dB with 1 dB resolution and treble is adjustable between +12 dB with 1 dB resolution.

For the purpose of a simple control software in the microcontroller, the decimal number that is sent as an I^2C-bus data byte for bass or treble is identical to the new bass or treble setting in dB (e.g. the 12C-bus data byte +8 sets the new value to +8 dB).

The beeper provides tones in a range from approximately 400 Hz to 30 kHz. The frequency can be selected via the I^2C-bus. The beeper output signal is added to the loudspeaker and headphone channel signals. The beeper volume is adjustable with respect to full scale between 0 and -93 dB with 3 dB resolution. The beeper is not effected by mute.

Soft mute provides a mute ability in addition to volume control with a well defined time (32 ms) after which the soft mute is completed. A smooth fading is achieved by a cosine masking.

6.2.6 FEATURE INTERFACE

The feature interface comprises two I^2S-bus input/output ports and a system clock output. Each I^2S-bus port is equipped with level adjust facilities that can change the signal level in a range of ±15 dB with 1 dB resolution.

Outputs can be disabled to improve EMC performance. The I^2S-bus output matrix provides the following functions; forced mono, stereo, channel swap, channel 1 and channel 2.

One example of how the feature interface can be used in a TV set is to connect an external Dolby Surround Pro Logic DSP, such as the SAA7710, to the I^2S-bus ports. Outputs must be enabled and a suitable master clock signal for the DSP can be taken from pin SYSCLK.

A stereo signal from any source will be output on one of the I^2S-bus serial data outputs and the four processed signal channels will be entered at both I^2S-bus serial data inputs. Left and right could then be output to the power amplifiers via the Main channel, centre and surround via the Auxiliary channel.

6.2.7 CHANNEL FROM THE AUDIO ADC

The signal level at the output of the ADC can be adjusted in a range of ±15 dB with 1 dB resolution. The audio ADC itself is scaled to a gain of -6 dB.

6.2.8 CHANNEL TO THE ANALOG CROSSBAR PATH

Level adjust with control positions 0 dB, +3 dB, +6 dB and +9 dB.

6.2.9 DIGITAL CROSSBAR SWITCH (See Fig.6)

Input channels to the crossbar switch are from the audio ADC, I^2S1, I^2S2, FM path and from the loudspeaker channel path after matrix and AVL.

Output channels comprise loudspeaker, headphone, I^2S1, I^2S2 and the audio DACs for line output and SCART.

The I^2S1 and I^2S2 outputs also provide digital outputs from the loudspeaker and headphone channels, but without the beeper signals.

6.2.10 GENERAL

There are a number of functions that can provide signal gain, e.g. volume, bass and treble control. Great care has to be taken when using gain with large input signals in order not to exceed the maximum possible signal swing, which would cause severe signal distortion. The nominal signal level of the various signal sources to the digital crossbar switch should be 15 dB below digital full scale (15 dB full scale). This means that a volume setting of, say, +15 dB would just produce a full scale output signal and not cause clipping, if the signal level is nominal.

Sending illegal data patterns via the I^2C-bus will not cause any changes of the current setting for the volume, bass, treble, bass boost and level adjust functions.

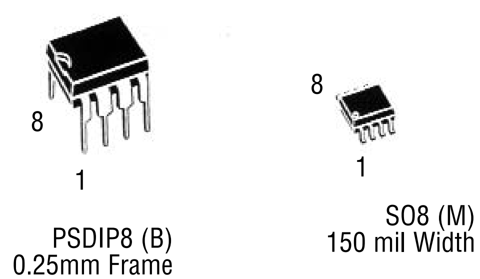
6.2.11 EXPERT MODE

The TDA9870A provides a special expert mode that gives direct write access to the internal Coefficient RAM (CRAM) of the DSP. It can be used to create user-defined characteristics, such as a tone control with different corner frequencies or special boost/cut characteristics to correct the low-frequency loudspeaker and/or cabinet frequency responses by means of the bass boost filter. However, this mode must be used with great care.

More information on the functions of this device, such as the number of coefficients per function, their default values, memory addresses, etc., can be made available

ST24C16, ST25C16, ST24W16, ST25W16
Serial 16 K (2K x 8) Eeprom

- **1 million erase/write cycles, with 40 years data retention**
- **Single supply voltage:**
  - 4.5V to 5.5V for ST24x16 versions
  - 2.5V to 5.5V for ST25x16 versions
- **Hardware write control versions:** ST24W16 and ST25W16
- **Two wire serial interface, fully I2C Bus compatible**
- **Byte and Multibyte write** (up to 8 bytes) for the ST24C16
- **Page write** (up to 16 bytes)
- **Byte, random and sequentıal read modes**
- **Self timed programming cycle**
- **Automatic address incrementing**
- **Enhanced ESD/Latch up performances**



DESCRIPTION

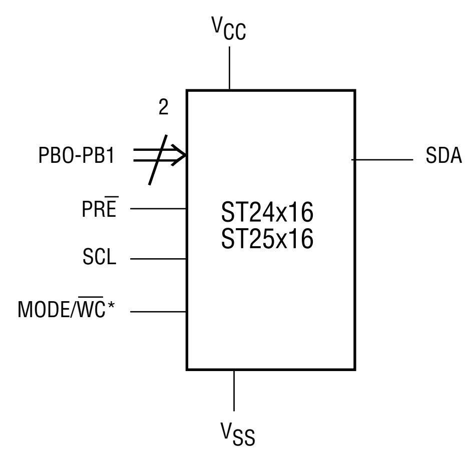
This specification covers a range of 16K bits I2C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where “X” is: “C” for Standard version and “W” for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256 x 8 bits. These are manufactured in SGS-Thomson’s Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 40 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are Available.

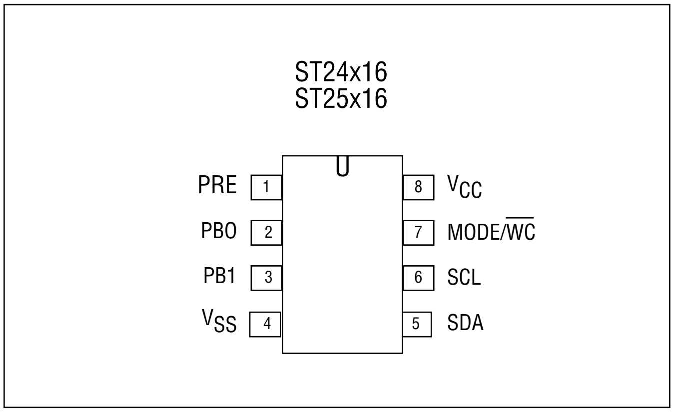
Table 1. Signal Names

PRE	Write Protect Enable
PB0, PB1	Protect Block Select
SDA	Serial Data Address Input/Output
SCL	Serial Clock
MODE	Multybyte/Page Write Mode (C version)
$\overline{WC}$	Write Control (W version)
Vcc	Supply Voltage
Vss	Ground

Figure 1. Logic Diagram



DIP Pin Connections



SO8 Pin Connections

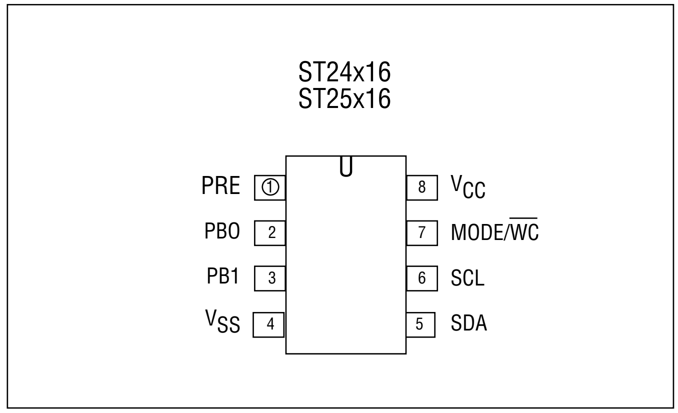


Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter			Value	Unit
T_A	Ambient Operating Temperature			-40 to 125	°C
T_{STG}	Storage Temperature			-65 to 150	°C
T_{LEAD}	Lead Temperature, Soldering	(SO8)	40 sec	215	°C
		(PSDIP8)	10 sec	260	°C
V_{IO}	Input or Output Voltage			-0.6 to 6.5	V
V_{CC}	Supply Voltage			-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body Model) [2]			4000	V
	Electrostatic Discharge Voltage (Machine Model) [3]			500	V

Notes: 1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.
2. 100pF through 1500Ω; MIL-STD-883C, 3015.7
3. 200pF through 0Ω; EIAJ IC-121 (condition C)

DESCRIPTION

The memories are compatible with the I2C standard two wire serial interface which uses a bi-directional data bus and serial clock. The memories carry a built-in 4 bit, unique device identification code (1010) corresponding to the I2C bus definition. The memories behave as slave devices in the I2C protocol with all memory with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge bit. When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition .

TDA8351

DC-coupled vertical deflection circuit

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short - circuit of the output pins (7 and 4)
  - short - circuit of the output pins to Vp
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A quard signal in zoom mode.

GENERAL DESCRIPTION

The TDA8351 is a power circuit for use in 90° and 100° colour deflection systems for field frequencies of 50 to 120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system.

QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
DC supply						
V_P	supply voltage		9	-	25	V
I_q	quiescent supply current		-	30	-	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		-	-	3	A
$I_{diff(p-p)}$	differential input current (peak-to-peak value)		-	600	-	µA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		-	1.5	1.8	V
Flyback switch						
I_M	peak output current		-	-	±1.5	A
V_{FB}	flyback supply voltage		-	-	50	V
		note 1	-	-	60	V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		-55	-	+150	°C
T_{amb}	operating ambient temperature		-25	-	+75	°C
T_{vj}	virtual junction temperature		-	-	150	°C

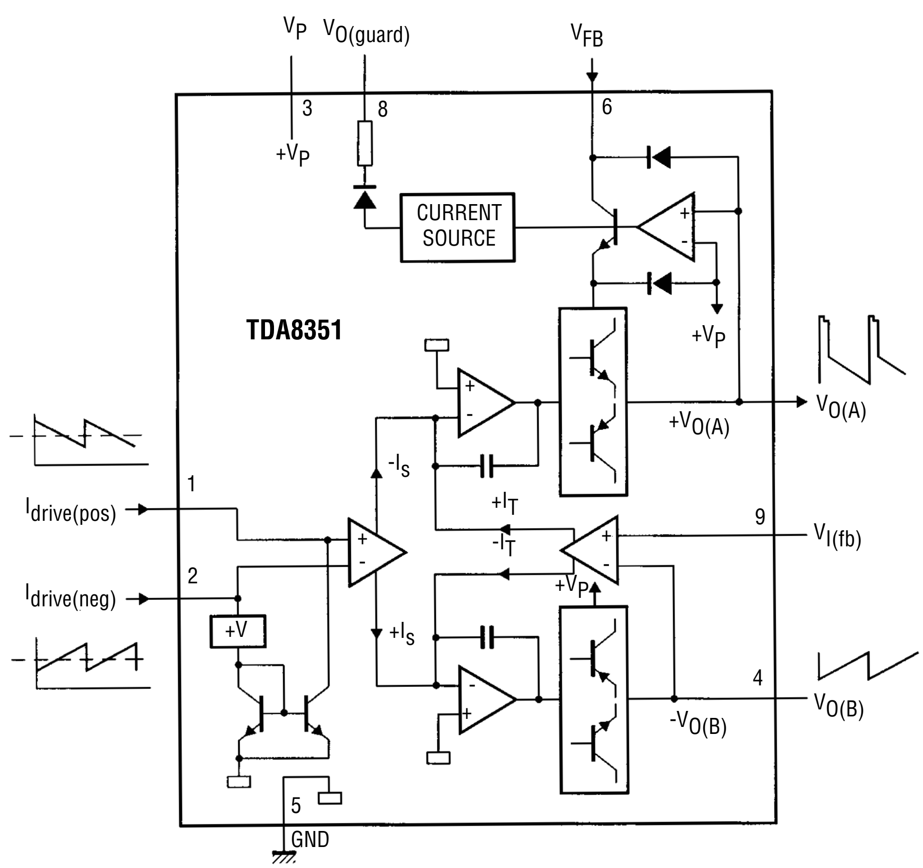
Note:

1- A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.G).

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8351	SIL9P	plastic single-in-line power package; 9 leads	SOT131-2

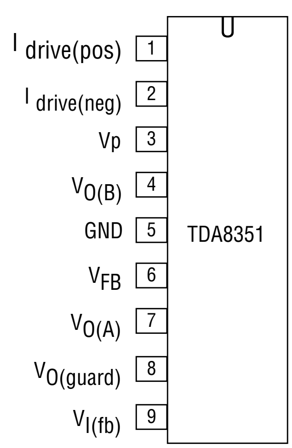
Block Diagram



PINNING

SYMBOL	PIN	DESCRIPTION
$I_{drive(pos)}$	1	input power-stage (positive); includes $I_{I(sb)}$ signal bias
$I_{drive(neg)}$	2	input power-stage (negative); includes $I_{I(sb)}$ signal bias
Vp	3	operating supply voltage
$V_{O(B)}$	4	output voltage B
GND	5	ground
V_{FB}	6	input flyback supply voltage
$V_{O(A)}$	7	output voltage A
$V_{O(guard)}$	8	guardoutput voltage
$V_{I(fb)}$	9	input feedback voltage

Pin Configuration



Metal block connected to substrate pin 5.
Metal on back

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (RM) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150A, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (RCON) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying RM. The maximum input differential voltage is 1.8 V. In the application it is recommended that V_{diff} = 1.5 V (typ), This is recommended because of the spread of input current and the spread in the value of R_{CON}

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage Vp optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to Vp.

  A guard circuit $V_{O(guard)}$ is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to Vp or ground
- during open loop
- when the thermal protection is activated.

  This signal can be used for blanking the picture tube screen.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEJ 134)

Symbol	Parameter	Conditions	Min.	Max.	Unit
DC supply					
V_P	supply voltage	non-operating	-	40	V
			-	25	V
V_{FB}	flyback supply voltage		-	50	V
		note 1	-	60	V
Vertical circuit					
$I_{O(p\text{-}p)}$	output current (peak-to-peak value)	note 2	-	3	A
$V_{O(A)}$	output voltage (pin 7)		-	52	V
		note 1	-	62	V
Flyback switch					
I_M	peak output current		-	±1.5	A
Thermal data (in accordance with IEC 747-1)					
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		-25	+75	°C
T_{vj}	virtual junction temperature		-	150	°C
$R_{th\ vj\text{-}c}$	resistance v_j-case		-	4	K/W
$R_{th\ vj\text{-}a}$	resistance v_j-ambient in free air		-	40	K/W
Tsc	short-circuiting time	note 3	-	1	hr

Notes:

1. A flyback supply voltage of >50 V up to 60 V is allowed in application. A 220 nF capacitor in series with a 22Ω resistor (dependent on I_O and the inductance of the coil) has to be connected between pin 7 and ground. The decoupling capacitor of V_{FB} has to be connected between pin 6 and pin 3. This supply voltage line must have a resistance of 33 Ω (see application circuit Fig.6).
2. I_O maximum determined by current protection.
3. Up to Vp = 18V.

TDA2616

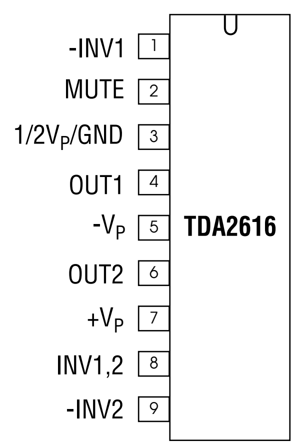
2x12W Hi-Fi Audio Power Amplifiers with Mute

GENERAL DESCRIPTION

The TDA2616 is a dual power amplifiers. It has been especially designed for mains fed applications such as stereo radio and stereo TV.

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-Fi accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.



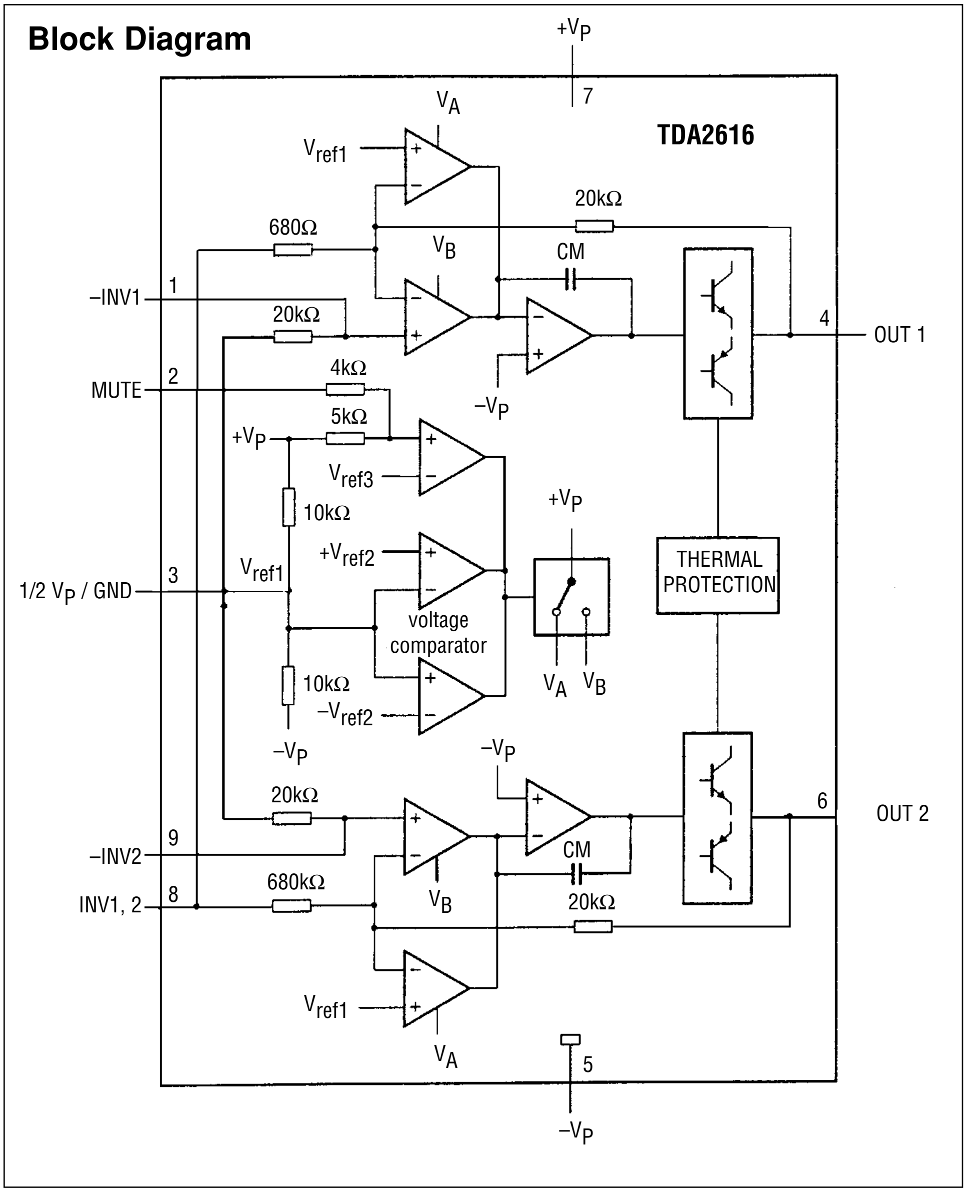
Pin Configuration

PINNING

Pin	Symbol	Function
1	-INV1	non-inverting input 1
2	MUTE	mute input
3	$1/2V_P$/GND	1/2 supply voltage or ground
4	OUT1	output 1
5	$-V_P$	supply voltage (negative)
6	OUT2	output 2
7	$+V_P$	supply voltage (positive)
8	INV1,2	inverting inputs 1,2
9	-INV2	non-inverting input 2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
$\pm V_P$	supply voltage range		7.5	-	21	V
P_0	output power	$V_P = \pm 16V$; THD = 0.5%	-	12	-	W
G_V	internal voltage gain		-	30	-	dB
I G_V I	channel unbalance		-	0.2	-	dB
α	channel separation		-	70	-	dB
SVRR	supply voltage ripple rejection		-	60	-	dB
V_{no}	noise output voltage		-	70	-	µV



LIMITING VALUES

In accordance with the Absolute maximum System (IEC 134)

Symbol	Parameter	Conditions	Min.	Max.	Unit
$\pm V_P$	supply voltage		-	21	V
I_{OSM}	non-repetitive peak output current		–	4	A
P_{tot}	total power dissipation		–	25	W
T_{stg}	storage temperature range		–55	+150	°C
T_{XTAL}	crystal temperature		–	+150	°C
T_{amb}	ambient operating temperature range		–25	150	°C
Tsc	short circuit time	short-circuit to ground; note 1	–	1	h

Note to the limiting values

1. For asymmetrical power supplies (with the load short-circued), the maximum unloaded supply voltage is limited to V_P = 28 V and with an internal supply resistance of $R_S \geq 4\Omega$, the maximum unloaded supply voltage is limited to 32 V (with the load short-circuited). For symmetrical power supplies the circuit is short-circuit-proof up to V_P=±21V.

TDA7057AQ

2 x5 W stereo BTL Audio Output Amplifier with DC Volume Control

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057AQ is astereo BTL output amplifier with DC volume control. The device is designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

Missing Current Limiter (MCL)

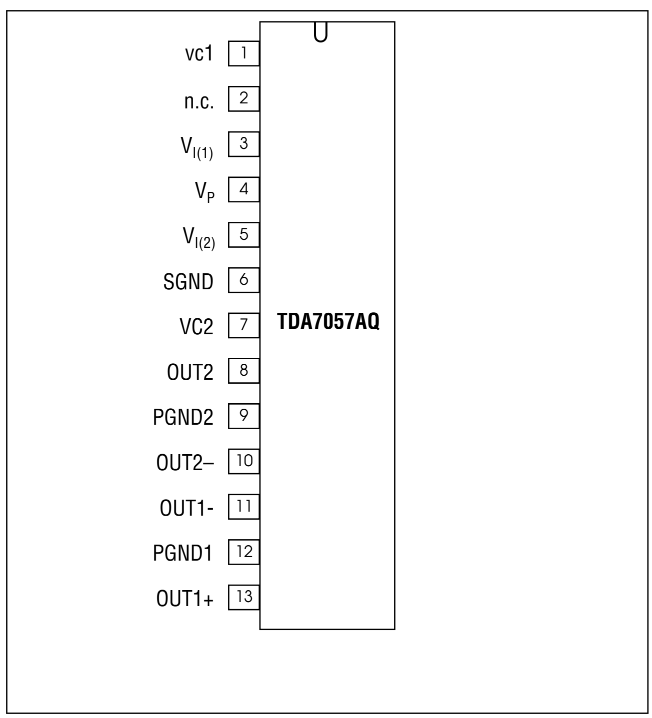
A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

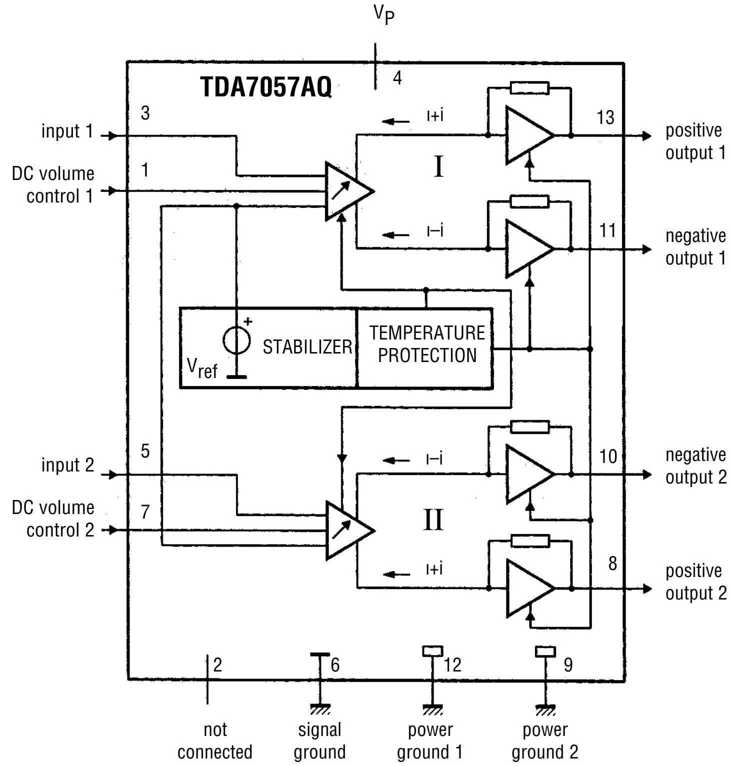
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	–	18	V
P_{out}	output power	V_p = 12 V; R_L = 16 Ω	3.0	3.5	–	W
		V_p = 12 V; R_L = 8Ω	–	5.3	–	W
G_v	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68.0	73.5	–	dB
$I_{q(tot)}$	total quiescent current	V_p = 12 V; R_L = ∞	–	22	25	mA
THD	total harmonic current	P_{out}=0.5w w	–	0.3	1	%

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA7057AQ	DBS13P	Plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)	SOT141-6

SYMBOL	PIN	DESCRIPTION
VC1	1	DC volume contol 1
n.c.	2	not connected
$V_{I\,(1)}$	3	voltage input 1
V_P	4	positive supply voltage
$V_{I\,(2)}$	5	voltage input 2
SGND	6	signal ground
VC2	7	DC volume contol 2
OUT2+	8	positeve output 2
PGND2	9	power ground 2
OUT2-	10	negative output 2
OUT1-	11	negative output 1
PGND1	12	powwer ground 1
OUT1+	13	positive output 1





Block diagram

FUNCTIONAL DESCRIPTION

The TDA7057AQ is a stereo output amplifiers with two DC volume control stages. The device is designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

In the TDA7057AQ the two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages:

• Lower peak value of the supply current

• The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions.

For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 dB to -33 dB. If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit protected to ground, Vp and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above 150 oC the gain will be reduced, thereby reducing the output power.

Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

TDA7050

Low voltage mono/stereo power amplifier

GENERAL DESCRIPTION

The TDA7050 is a low voltage audio amplifier for small radios with headphones (such as watch, pen and pocket radios) in mono (bridge-tied load) or stereo applications.

FEATURES

• Limited to battery supply application only (typ. 3 and 4 V)
• Operates with supply voltage down to 1.6 V
• No external components required
• Very low quiescent current
• Fixed integrated gain of 26 dB, floating differential input
• Flexibility in use - mono BTL as well as stereo
• Small dimension of encapsulation (see package design example)

QUICK REFERENCE DATA

Supply voltage range	Vp	1.6 to 6.0V	
Total guiescent current (at V_p = 3V)	Itot	typ.	3.2 mA
Bridge tied load application (BTL)			
Output power at RL = 32Ω			
V_p = 3V; d_{tot} = 10%	Po	TYP.	140 mW
D.C. output offset voltage between the outputs	ΔV	max	70 mV
noise output voltage (r.m.s. value)			
at f = 1 kHz; R_S = 5Ω	Vno(rms)	typ.	140µV
Stereo applications			
Output power at R_L = 32Ω			
d_{tot} =10%; V_p = 3V	Po	typ.	35 mW
d_{tot} =10%; V_p = 4.5V	Po	typ.	75mW
Channel separation at Rs = 0Ω; f = 1 kHz	α	typ.	40 dB
noise output voltage (r.m.s. value)			
at f = 1 kHz; R_S = 5Ω	Vno(rms)	typ.	100µV

PACKAGE OUTLINE

8 -lead DIL; plastic (SOT97); SOT97-1; 1996 July 23.

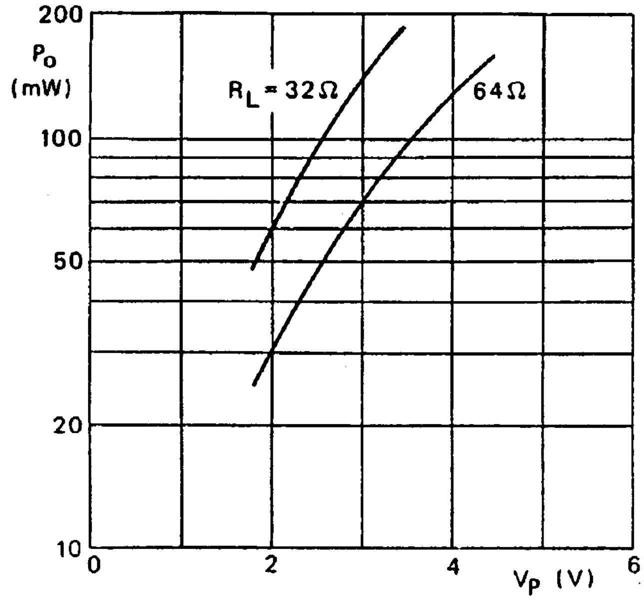


Fig. 2 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in BTL application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25°C

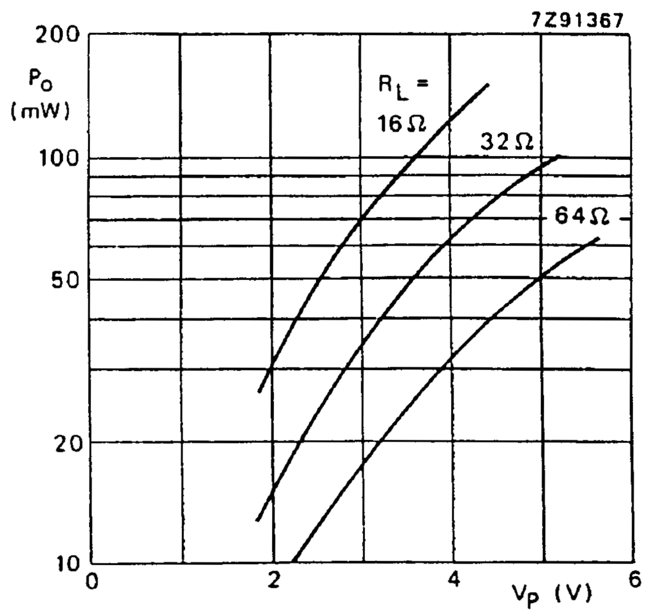


Fig. 3 Output power across the load impedance (R_L) as a function of supply voltage (V_P) in stereo application. Measurements were made at f = 1 kHz; d_{tot} = 10%; T_{amb} = 25°C

CHARACTERISTICS

V_p = 3V; f = 1 kHz; R_L = 32 Ω; T_{amb} = 25 °C; unless otherwise specified

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	Vp	1.6	–	6.0	V
Total guiescent current	Itot	–	3.2.	4	mA
Bridge tied load application (BTL); see Fig.4					
Output power; note 1					
V_p = 3.0V; d_{tot} = 10%	P_o	–	140	–	mW
V_p = 4.5V; d_{tot} = 10% (R_L = 64Ω)	P_o	–	150	–	mW
Voltage gain	G_v	–	32	–	dB
Noise output voltage (r.m.s. value)					
R_S = 5Ω; f = 1 kHz;	$V_{no(rms)}$	–	140	–	µV
R_S = 0Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	µV
D.C. output offset voltage (at R_S = 5Ω)	$\lvert \Delta V \rvert$	–	–	70	mV
input impedance (at Rs = ∞)	$\lvert Z_i \rvert$	–	–	–	MΩ
input bias current	I_i	–	40	–	nA
Stereo applications; see Fig 5					
Output power; note 1					
V_p = 3.0V; d_{tot} = 10%	P_o	–	35	–	mW
V_p = 4.5V; d_{tot} = 10%	P_o	–	75	–	mW
Voltage gain	G_v	24.5	26	27.5	dB
Noise output voltage (r.m.s. value)					
R_S = 5Ω; f = 1 kHz;	$V_{no(rms)}$	–	100	–	µV
R_S = 0Ω; f = 500 kHz; B = 5 kHz	$V_{no(rms)}$	–	tbf	–	µV
Channel separation					
Rs = 0Ω; f = 1 kHz	α	30	40	–	dB
input impedance (at Rs = ∞)	$\lvert Z_i \rvert$	2	–	–	MΩ
input bias current	I_i	–	20	–	nA

Note

1.Output power is measured directly at the output pins of the IC. It is shown as a function of the supply voltage in Fig. 2 (BTL application) and Fig. 3 (stereo application).

TDA6107Q

Triple video output amplifier

FEATURES

- Typical bandwidth of 5.5 MHz for an output signal of 60 V (peak-to-peak value)
- High slew rate of 900 V/µs
- No external components required
- Very simple application
- Single supply voltage of 200 V
- Internal reference voltage of 2.5 V
- Fixed gain of 50
- Black-Current Stabilization (BCS) circuit
- Thermal protection.

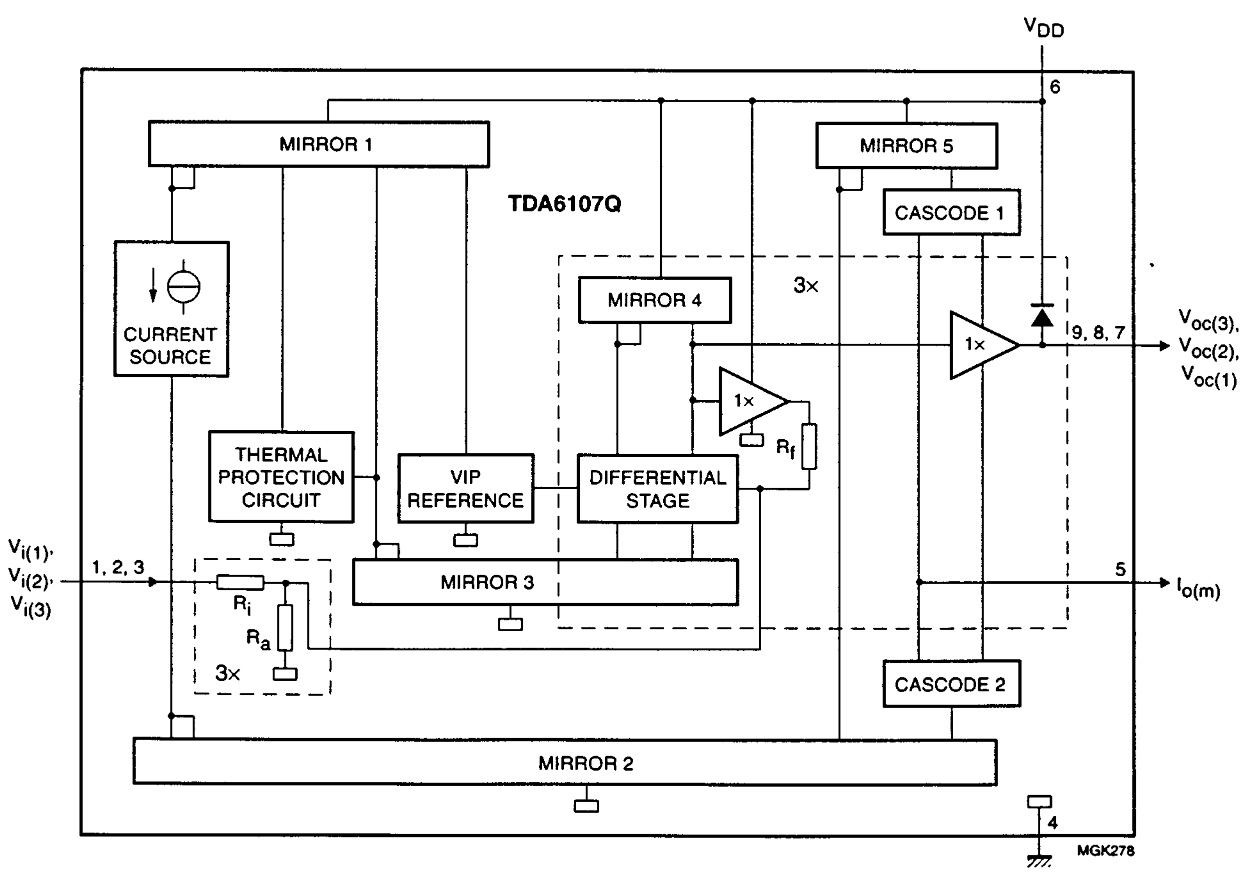
GENERAL DESCRIPTION

The TDA6107Q includes three video output amplifiers in one plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1), using high-voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black -current control.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6107Q	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

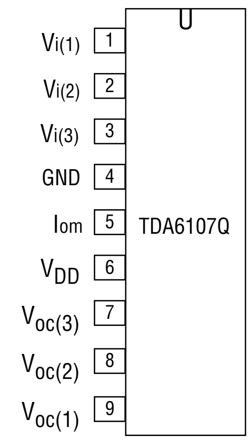
Block Diagram



PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

Pin Configuration



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages measured with respect to pin 4 (ground); currents as specified in Fig. 1; unless otherwise specified.

No	Symbol	Parameter	Min.	Max.	Unit
101	V_{DD}	supply voltage	0	250	V
102	V_i	input voltage at pins 1 to 3	0	12	V
103	$V_{o(m)}$	measurement output voltage	0	6	V
104	$V_{o(c)}$	cathode output voltage	0	V_{DD}	V
107	T_{stg}	storage temperature	-55	+150	°C
108	T_j	junction temperature	-20	+150	°C
	Ves	electrostatic handling			
109		Human Body Model (HBM)	-	2000	V
110		Machine Model (MM)	-	300	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see “Handling MOS Devices”).

QUALITY SPECIFICATION

Quality specification “SNW-FQ-611 part D” is applicable and can be found in the “Quality reference Handbook”.

The handbook can be ordered using the code 9397 750 00192.

TCDT1100(G) Series
Optocoupler with Phototransistor Output

FEATURES

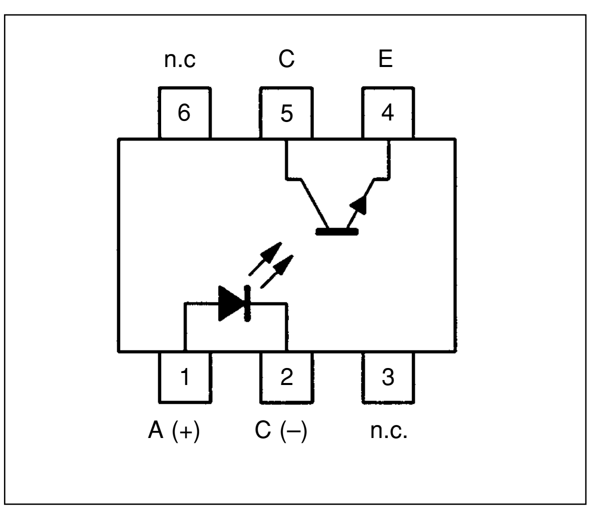
According to VDE 0884:
- Rated impulse voltage (transient overvoltage)
  VIOTM = 6 kV peak
- Isolation test voltage (partial discharge test voltage)
  Vpd = 1.6 kV
- Rated isolation voltage (RMS includes DC)
  VIOWM = 600 VRMS (848 V peak)
- Rated recurring peak voltage (repetitive)
  VIoRM = 600 VRMS
- Creepage current resistance according to
  VDE 0303/1EC 112
  Comparative Tracking Index: CTI = 275
- Thickness through insulation ≥ 0.75 mm
- Further approvals:
  BS 415, BS 7002, SETI: IEC 950,
  UL 1577: File No: E 76222
- Base not connected
- CTR offered in 4 groups
- Isolation materials according to UL94-VO
- Pollution degree 2 (DIN/VDE 0110 / resp. IEC 664)
- Climatic classification
  55/100/21 (IEC 68 part 1)
- Special construction:
  Therefore extra low coupling capacity of typical
  0.2 pF, high Common Mode Rejection
- Low temperature coefficient of CTR

ORDER SCHEMATIC

PART NUMBERS	CTR-RANKING
TCDT1100/TCDT1100G	>40%
TCDT1101/TCDT1101G	40 to 80%
TCDT1102/TCDT1102G	63 to 125%
TCDT1103/TCDT1103G	100 to 2000%

Suffix: G = Leadform 10.16 mm

Pin Connection



ABSOLUTE MAXIMUM RATINGS

Input (Emitter)

Parameters	Test Conditions	Symbol	Value	Unit
Reverse voltage		V_R	5	V
Forward current		I_F	60	mA
Forward surge current	$t_p \leq 10\mu s$	I_{FSM}	3	A
Power dissipation	$T_{amb} \leq 25$ °C	P_v	100	mW
Junction temperature		T_j	125	°C

Output (Detector)

Parameters	Test Conditions	Symbol	Value	Unit
Collector emitter voltage		V_{CEO}	32	V
Emitter collector voltage		V_{ECO}	7	V
Collector current		I_C	50	mA
Collector peak current	$t_p/T = 0.5$, $t_p \leq 10ms$	I_{CM}	100	mA
Power dissipation	$T_{amb} \leq 25$ °C	P_v	150	mW
Junction temperature		T_j	125	°C

Coupler

Parameters	Test Conditions	Symbol	Value	Unit
Isolation test voltage (RMS)		V_{IO}	3.75	kV
Total power dissipation	$T_{amb} \leq 25$ °C	P_{tot}	250	mW
Ambient temperature range		T_{amb}	-55 to +100	°C
Storage temperature range		T_{stg}	-55 to +125	°C
Soldering temperature	2 mm from case $t \leq 10$ s	T_{sd}	260	°C

TDA9830

TV sound AM-demodulator and audio source switch

FEATURES

- Adjustment free wideband synchronous AM demodulator
- Audio source-mute switch (low noise)
- Audio level according EN50049
- 5 to 8 V power supply or 12 V alternative
- Low power consumption.

GENERAL DESCRIPTION

The TDA9830, a monolithic integrated circuit, is designed for AM-sound demodulation used in L- and L'-standard.
The IC provides an audio source selector and also mute switch.

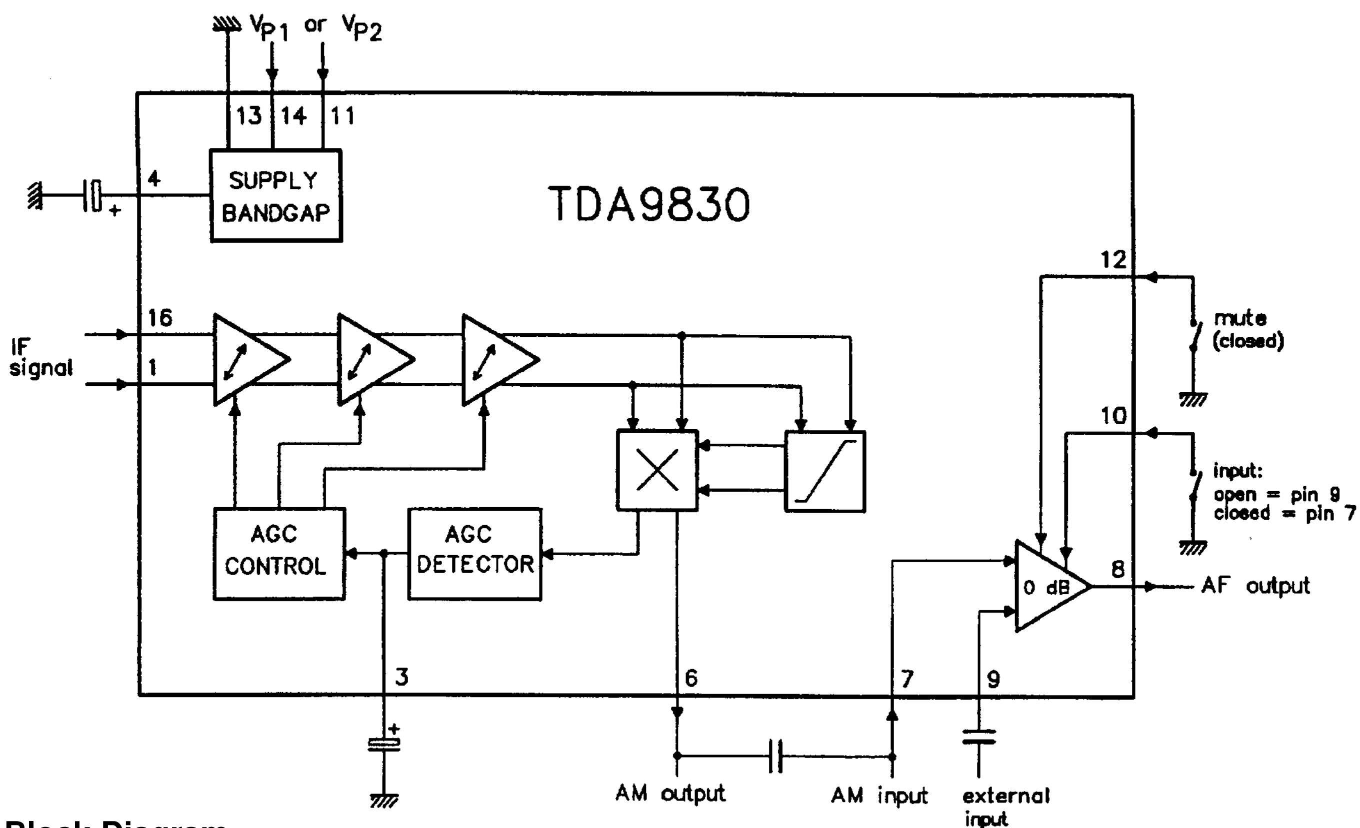
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT
V_{14}	positive supply voltage	4.5	5.0	8.8	V
V_{11}	supply voltage (alternative)	10.8	12.0	13.2	V
I14,11	supply current	24	30	36	mA
V_{1-16}	IF sensitivity (RMS value) (for -3 dB AF-signal)	-	60	100	μV
G_v	gain control	60	66	-	dB
V_6	AF output signal (m - 54%) (RMS value)	400	500	600	mV
Vs	S/N ratio ace. CCIR468-3 (IF-signal 10 mV_{RMS})	47	53	-	dB
$V_{7,9}$	AF input signal (for THD < 1.5%) (RMS value)	-	-	1.2	V
V_8	crosstalk and mute attenuation	80	90	-	dB
T_{amb}	operating ambient temperature	0	-	+70	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA9830	16	DIL	plastic	SOT38GG(1)
TDA9830T	16	SO	plastic	SOT109(2

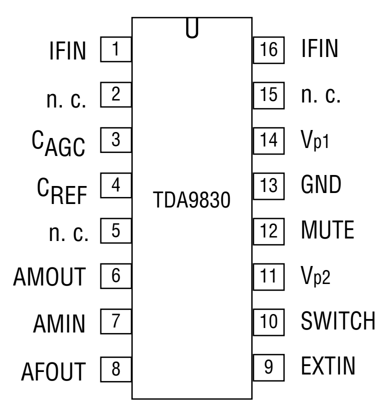
Note
1. SOT38-1; 1996 November 20.
2. SOT109-1 1996 Novembe r20.



Block Diagram

PINNING

SYMBOL	PIN	DESCRIPTION
IFIN	1	sound IF differential input signal
n.c.	2	not connected
C_{AGC}	3	AGC capacitor
C_{REF}	4	REF voltage filtering capacitor
n.c.	5	not connected
AMOUT	6	AM demodulator output
AMIN	7	input signal (from AM) to audio switch
AFOUT	8	output signal from audio switch
EXTIN	9	input signal (from external) to audio switch
SWITCH	10	switch input select control
V_{p2}	11	supply voltage +12 V (alternative)
MUTE	12	mute control
GND	13	ground (0 V)
V_{p1}	14	supply voltage +5 to +8 V
n.c.	15	not connected
IFIN	16	sound IF differential input signal



Pin configuration

CHARACTERISTICS

V_{p1} = 5.0 V at pin 14; T_{amb} = +25 °C; sound carrier f_{SC} = 32.4 MHz modulated with f = 1 kHz and modulation depth m = 54%. IF input signal (sound carrier): V_{1-16} 10 mV_{RMS}; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{14-13}	positive supply voltage Vp1	note 1	4.5	5.0	8.8	V
V_{11-13}	positive supply voltage Vp2	note 1	10.8	12.0	13.2	V
I_{11}/I_{14}	current consumption		24	30	36	mA
IF amplifier and gain control						
R_{1-16}	input resistance		1.75	2.2	2.65	kΩ
C_{1-16}	input capacitance		1.0	1.5	2.2	pF
V_{1-16}	minimum IF input signal (RMS value)	note 2	–	60	100	µV
V_{1-16}	maximum IF input signal (RMS value)	note 3	70	120	–	mV
G_V	gain control		60	66	–	dB
I_3	maximum AGC charging/discharging current	3.5	5	7	µA	
I_3	fast AGC discharging current		–	–	5	mA
V_3 - V_{13}	gain control voltage (G_{min} - G_{max})		1.5	–	2.8	V
B	–3dB IF bandwidth	upper cut-off frequency	50	70	–	MHz
		lower cut-off frequency	–	6	10	MHz
$V_{1/16-13}$	DC potential		–	1.7	–	V
AM-Demodulator						
V_{6-13}	AF output signal (RMS value)		400	500	600	mV
B	-3 dB AF bandwidth	upper cut-off frequency	100	–	–	kHz
		lower cut-off frequency; note 7	–	–	20	Hz
V_{6-13}	THD		–	0.8	2	%
V_{6-13}	S/N (weighted acc. CCIR 468-3)		47	53	–	dB
V_{6-13}	DC potential		2.00	2.15	2.30	V
R_6	output resistance (emitter follower with 0.5 mA bias current)		–	300	–	Ω
I_{6abs}	allowable AC output current		–	–	0.3	mA
I_6	allowable DC output current		–	–	0.5	mA
Audio-switch						
$V_{7,9-13}$	AF-input-signal for THD < 1.5% (RMS value)		–	–	1.2	V
V_{8-13}	S/N ratio of audio switch (in accordance with CCIR 468-3)	reference signal at pin 7/9 is 0.5 V_{RMS}	70	80	–	dB
B	-3 dB AF bandwidth	upper limit	100	–	–	kHz
V_{8-13}	THD at 1 V_{RMS} input signal at pin 7 or 9		–	0.1	1.0	%
V_{8-13}	crosstalk and mute attenuation	20 Hz to 20 kHz	80	90	–	dB
$V_{7,8,9-13}$	DC-potential		2.00	2.15	2.30	V
$R_{7,9-13}$	input resistance		40	50	60	kΩ
$G_{7,9-8}$	gain of audio switch		-0.5	0	+0.5	dB
V_{10-13}	audio switching voltage to activate pin 7		0	–	0.8	V
V_{10-13}	audio switching voltage to activate pin 9	note 4	1.5	–	Vp	V

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{12-13}	input voltage for MUTE-ON		0	–	0.8	V
	input voltage for MUTE-OFF	note 4	1.5	–	Vp	V
$I_{10, 12}$	output current of switching-pins at V 10,12-13= 0V		-110	-145	-185	μA
V_{8-13}	DC-plop at AF output pin with switching from internal to external audio signal or to mute-state or vice-versa	note 5	–	5	10	mV
R_8	output resistance		70	100	150	Ω
Ripple rejection note 6						
RR	AF signal output:		26	30	–	dB
	α_{RR} = V_{ripple} On Vp / V_{ripple} On V_{out} AF signal output with AF signal from externalsource		40	44	–	dB

Notes to the characteristics

1. *In the power supply voltage range Vpl = 5.0 V UP to 8.0 V the performance will not change essentially. With power supply from V_{p2} = 12.0 V the performance will be comparable with the performance at Vpl = 5•0 V UP fo 8.0 V.*
   The unused power supply pin must be not connected.
2. *Start of gain control (low IF input signal) at -3 dB AF signal reduction at pin 6.*
3. *End of gain control (high IF input signal) at +1 dB AF signal expansion at pin 6.*
4. *This state is also valid for pin left open-circuit.*
5. *If a DC-plop of about maximum 100 mV is acceptable when switching from internal to external audio-signal or from internal to mute state or vice versa, the capacitor between pin 6 and 7 can be omitted and pin 6 can be connected to pin 7.*
6. *Measured with V_{ripple} = 200 mV(p-p) at 70 Hz superimposed on supply voltage Vp.*
7. *Dependent on value of AGC capacitor.*

SAA7710T

Dolby Pro Logic Surround; Incredible Sound

FEATURES

- Two stereo I^2C-bus digital input channels
- Three stereo I^2C-bus digital output channels
- I^2C-bus mode control
- Up to 45 ms on-chip delay-line (fs = 44.1 kHz)
- Optional clock divider for crystal oscillator
- Package: SO32L
- Operating supply voltage range: 4.5 to 5.5 V.

Functions

- 4-channel active surround, 20 Hz to 20 kHz (maximum 1/2fs)
- Adaptive matrix
- 7 kHz low-pass filters
- Adjustable delay for surround channel
- Modified Dolby B noise reduction
- Noise sequencer
- Variable output matrix
- Sub woofer
- Centre mode control: on/off, normal, phantom, wide
- Output volume control
- Automatic balance and master level control with DC-offset filter
- Hall/matrix surround sound functions
- Incredible sound functions
- 5-band parametric equalizer on main channels left, centre, right (fs = 32 kHz)
- Tone control (bass/treble) on all four output channels (fs = 44.1 kHz).

GENERAL DESCRIPTION

This data sheet describes the 104 ROM-code version of the SAA7710T chip. The SAA7710T chip is a high quality audio-performance digital add-on processor for digital sound systems. It provides all the necessary features for complete Dolby Pro Logic surround sound on chip.

In addition to the Dolby Pro Logic surround function, this device also incorporates a 5-band parametric equalizer, a tone control section and a volume control. Instead of Dolby Pro Logic surround, the Hall/matrix surround and Incredible sound functions can be used together with the equalizer or tone control.

QUICK REFERENCE DATA

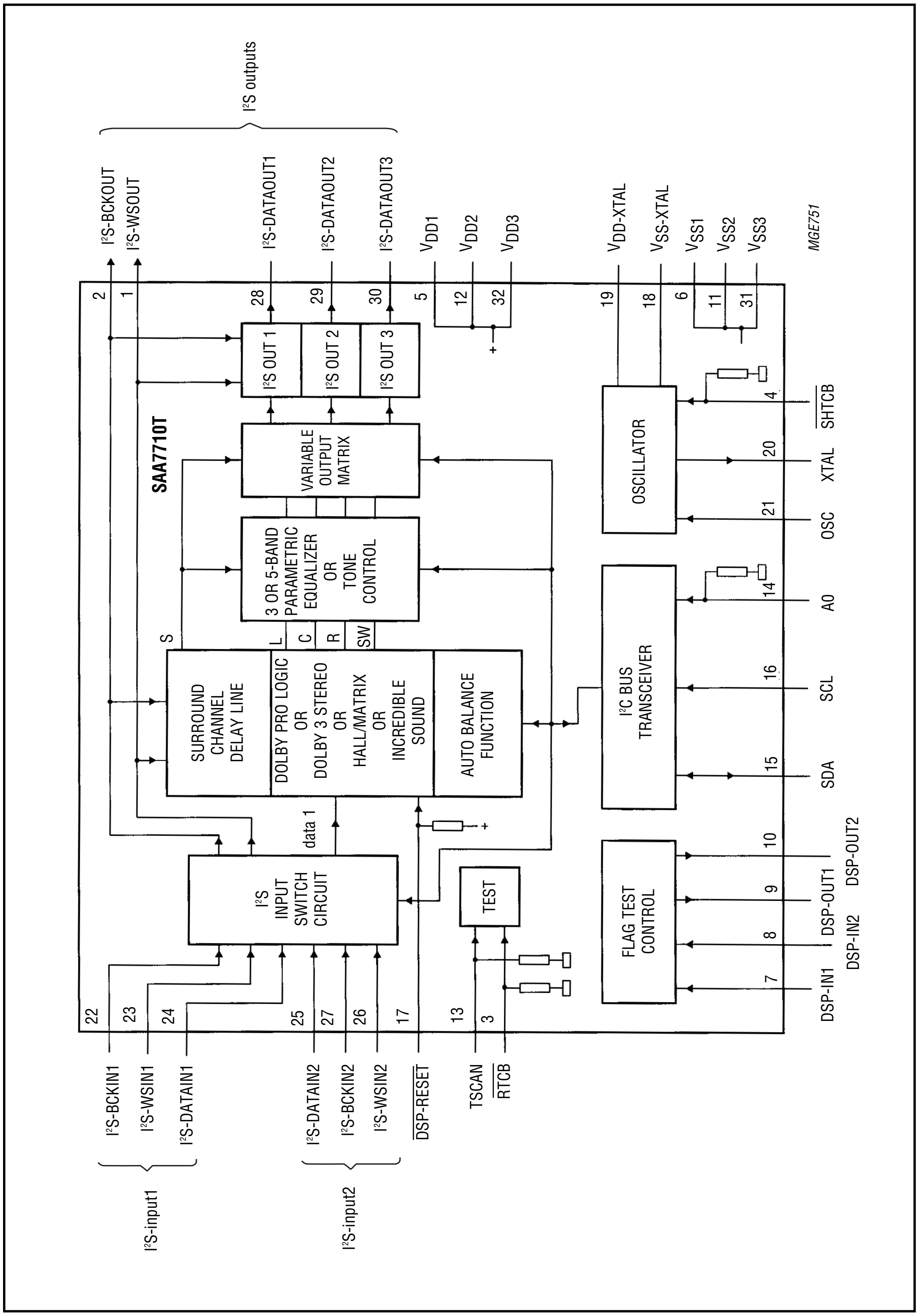
SYMBOL	PARAMETER	Min.	Max.	Unit
V_{DD}	DC supply voltage	-0.5	+6.5	V
ΔV_{DD}	voltage difference between two V_{DDx} pins	-	550	mV
V_i	Maximum input voltage	-0.5	V_{DD}+0.5	V
I_{DD}	DC supply current	-	50	mA
I_{ss}	DC supply current	-	50	mA
T_{amb}	ambient operating temperature	-40	+85	°C
T_{stg}	storage temperature range	-65	+150	°C

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ORDERING INFORMATION

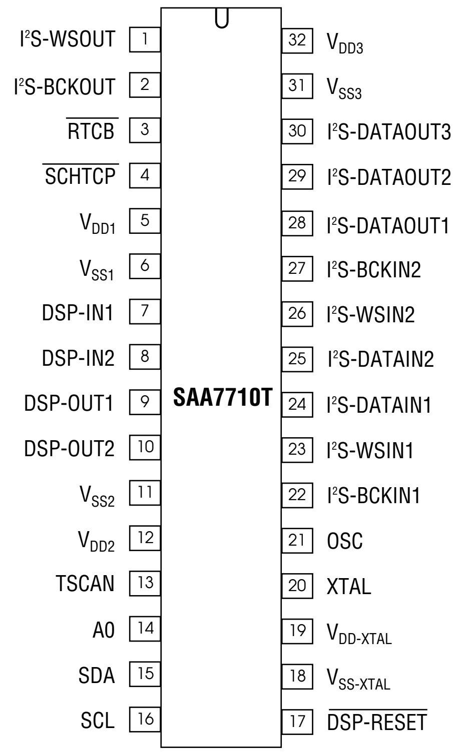
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7710T/N104	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

Block Diagram



PINNING

Symbol	Pin	Function
I^2S-WSOUT	1	I^2S-bus slave word-select output
I^2S-BCKOUT	2	I^2S-bus slave bit-clock output
$\overline{RTCB}$	3	asynchronous reset test control block input (active LOW)
$\overline{SHTCB}$	4	clock divider switch eneble input (LOW = divide)
V_{DD1}	5	positive power supply
V_{SS1}	6	ground power supply
DSP-IN1	7	flag input 1
DSP-IN2	8	flag input 2
DSP-OUT1	9	flag output 1
DSP-OUT2	10	flag output 2
V_{SS2}	11	ground power supply
V_{DD2}	12	positive power supply
TSCAN	13	scan control input
AO	14	I^2C-bus slave adress selection input
SDA	15	I^2C bus serial data input/output
SCL	16	I^2S-bus serial clock input
$\overline{DSP\text{-}RESET}$	17	chip reset input (active LOW)
$V_{SS\text{-}XTAL}$	18	ground power supply crystal oscillator
$V_{DD\text{-}XTAL}$	19	positive power supply crystal oscillator
XTAL	20	crystal oscillator output
OSC	21	crystal oscillator input
I^2S-BCKIN1	22	I^2S-bus master bit-clock input 1
I^2S-WSIN1	23	I^2S-bus master word-select input 1
I^2S-DATAIN1	24	I^2S-bus master data input 1
I^2S-DATAIN2	25	I^2S-bus master data input 2
I^2S-WSIN2	26	I^2S-bus master word-select input 2
I^2S-BCKIN2	27	I^2S-bus master bit-clock input 2
I^2S-DATAOUT1	28	I^2S-bus slave data output 1
I^2S-DATAOUT2	29	I^2S-bus slave data output 2
I^2S-DATAOUT3	30	I^2S-bus slave data output 3
V_{SS3}	31	ground power supply
V_{DD3}	32	positive power supply



Pin Configuration

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC134)

Symbol	Parameter	Conditions	Min.	Typ.	Unit
V_{DD}	DC supply voltage		-0.5	+6.5	V
ΔV_{DD}	voltage difference between two VDDx, pins		–	550	mV
$V_{i(max)}$	maximum input voltage		-0.5	V_{DD} + 0.5	V
I_{IK}	DC input clamp diode current	V_i < -0.5 V or V_i > V_{DD} + 0.5 V	–	10	mA
I_{OK}	DC output clamp diode current output type 4 mA	V_0 < -0.5 V or V_0 > V_{DD} + 0.5 V	–	20	mA
I_o	DC output source or sink current output type 4 mA	-0.5 V < V_0 < V_{DD} + 0.5 V	–	20	mA
I_{DD}	DC output source or sink current output type 4 mA	-0.5 V < V_0 < V_{DD} + 0.5 V	–	20	mA
I_{DD}	DC V_{DD} supply current per pin		–	50	mA
I_{SS}	DC V_{SS} supply current per pin		–	50	mA
V_{ESD}	ESD sensitivity for all pins human body model machine model all pins except pin OSC machine model pin OSC	 100 pF; 1500 Ω 200 pF; 2.5 µH; 0 Ω 200 pF; 2.5 µH; 0 Ω	 3000 300 250	 – – –	 V V V
LTCH	latch-up protection	CIC spec/test method	100	–	mA
P_{tot}	total power dissipation		–	700	mW
T_{amb}	operating ambient temperature		-40	+85	°C
T_{stg}	storage temperature		-65	+150	°C

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
Rth j-a	thermal resistance from junction to ambient in free air	57	K/W

DC CHARACTERISTICS

$V_{DD1} = V_{DD2} = V_{DD3} = V_{DD}$-XTAL = 4.5 to 5.5 V; T_{amb} = -40 to +85 °C; note 1; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDtot}	total DC supply voltage		4.5	5	5.5	V
$I_{DD(tot)}$	total DC supply current	DSP frequency=18 MHz; maximum activity DSP	-	50	55	mA
Ptot	total power dissipation	DSP frequency=18 MHz; maximum activity DSP	–	250	300	mW
V_{IH}	HIGH level input voltage all digital inputs and I/O_S	pin types 11, 12 and 13 pin type 14	$0.7V_{DDX}$ $0.8V_{DDX}$	– –	– –	V V
V_{IL}	LOW level input voltage all digital inputs and I/O_S	pin types 11, 12 and 13 pin type 14	– –	– –	$0.3V_{DDX}$ $0.2V_{DDX}$	V V
V_{hys}	hysteresis voltage	pin type 14	–	$0.33V_{DDX}$	–	V
V_{OH}	HIGH level output voltage digital outputs	V_{DDX} = 4.5 V; Io = -4 mA; pin type 01 and 02	4.0	–	–	V
V_{OL}	LOW level output voltage digital outputs	V_{DDX}=4.5 V; I_0 = 4 mA; pin types 13, 01 and 02	–	–	0.5	V
I_{LI}	input leakage current	V_i = O or V_{DDX} voltage; pin type I_1	–	–	1	µA
I_{LO}	output leakage current 3-state outputs	V_0 = O or V_{DDX} voltage; pin type 13 and O2	–	–	5	µA
$R_{pu(VDDX)(int)}$	internal pull-up resistor to V_{DDX}	pin type 14	17	–	134	kΩ
$R_{pd(VSSD)(int)}$	internal pull-down resistor to V_{SSD}	pin type I2	17	–	134	kΩ
Crystal oscillator						
V_{DDX}	positive supply voltage crystal oscillator		4.5	5	5.5	V

Note

1. $V_{DDX} = V_{DD-XTAL}$.

BU508AF

Silicon Diffused Power Transistor

GENERAL DESCRIPTION

High voltage, high-speed switching npn transistor in a fully isolated SOT199 envelope, primarily for use in horizontal deflection circuits of colour television receivers.

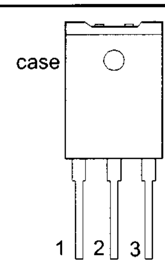
QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	700	V
I_C	collector current (DC)		–	8	A
I_{CM}	collector current peak value		–	15	A
P_{tot}	total power dissipation	$T_{hs} \leq 25$ °C	–	34	W
V_{CEsat}	collector - emitter saturation voltage	I_C = 4.5 A; I_B = 1.6 A	–	1.0	V
I_{Csat}	collector saturation current	f = 16kHz	4.5	–	A
t_f	fall time	I_{csat} = 4.5 A; f = 16kHz	0.7	–	µs

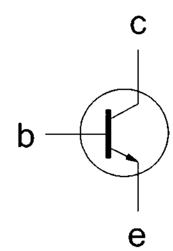
PINNING - SOT199

Pin	Description
1	base
2	collector
3	emitter
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	700	V
I_C	collector current (DC)		–	8	A
I_{CM}	collector current peak value		–	15	A
I_B	Base current (DC)		–	4	A
I_{BM}	Base current peak value		–	6	mA
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ °C	–	34	W
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction temperature		–	150	°C

THERMAL RESISTANCES

Symbol	Parameter	Conditions	Typ.	Max.	Unit
$R_{th\ j\text{-}hs}$	Junction to heatsink	without heatsink compound	–	3.7	K/W
$R_{th\ j\text{-}hs}$	Junction to heatsink	with heatsink compound	–	2.8	K/W
$R_{th\ j\text{-}a}$	Junction to ambient	in free air	35	–	K/W

ISOLATION LIMITING VALUE & CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H.≤ 65%; clean and dustfree	–		2500	V
C_{isol}	Capaticance from T2 to external heatsink	f= 1 MHz	–	22	–	pF

STATIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{ces}	Collector cut-off current [1]	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	–	–	1.0	mA
I_{ces}		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$ [2] T_j = 125 °C	–	–	2.0	mA
I_{EBO}	Emitter cut-off current	V_{EB} = 6.0 V; I_C = 0A	–	–	10	mA
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0A; I_c = 100 mA; L = 25 mH	700	–	–	V
V_{CEsat}	Collector-emitter saturation voltages	I_C = 4.5 A; I_B = 1.6 A;	–	–	1.0	V
V_{BEsat}	Base-emitter saturation voltages	I_C = 4.5 A; I_B = 2 A;	–	–	1.1	V
h_{FE}	DC current gain	I_C = 100 mA; V_{CE} = 5 V	6	13	30	

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
FT	Transition frequency at f= 5 MHz	Ic= 0.1 A; VCE = 5 V	7	–	MHz
C_c	Collector capacitance at f= 5 MHz	V_{CB} = 10V	125	–	pF
	Switching times (16 kHz line deflection circuit)	I_{Csat} = 4.5 A; L_c 1 mH;; C_{fb} = 4 nF $I_{B(end)}$ = 1.4 A; L_B = 6 µH; -V_{BB} = -4 V; -I_{BM} = 2.25A			
t_s	Turn-off storage time		6.5	–	µs
t_f	Turn-off fall time		0.7	–	µs

1 Measured with half sine-wave voltage (curve tracer)

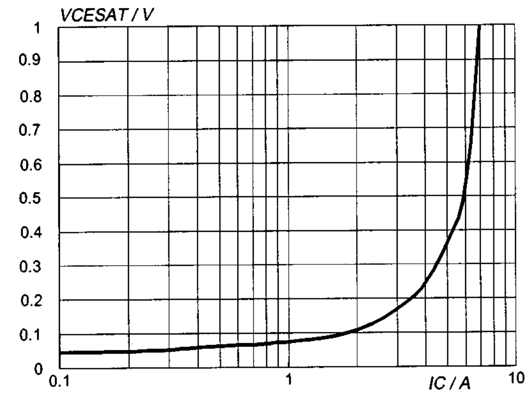


Fig. 7 Typical collector-emitter saturation voltage.
$V_{BE}sat = f(I_c)$; parameter I_C/I_B

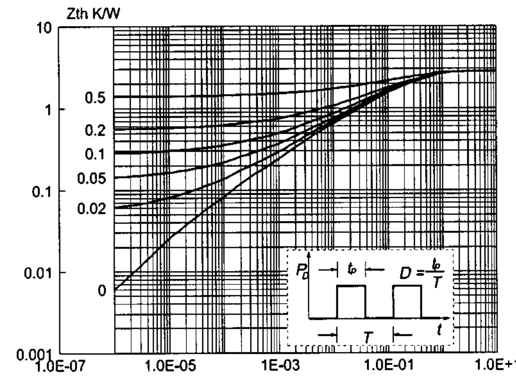


Fig. 10 Transient thermal impedance.
$Z_{th\ j\text{-}hs} = f(t)$; parameter $D = t_p/T$

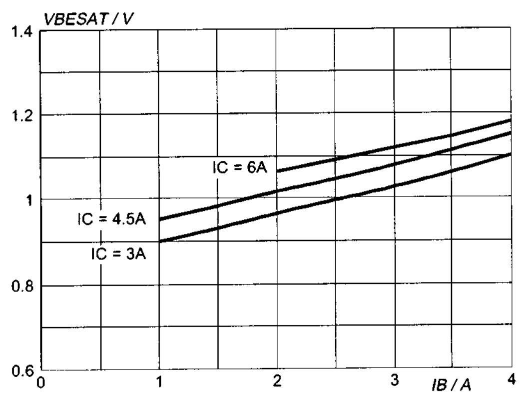


Fig. 8 Typical base - emitter saturation voltage.
$V_{BE}sat = f(I_B)$; parameter I_C

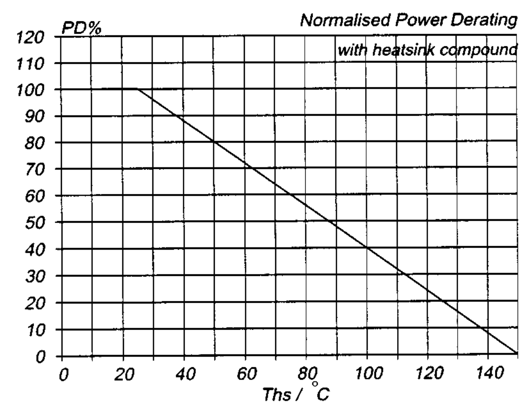


Fig. 11 Normalised power dissipation.
$PD\% = 100\ P_D/P_{D\ 25\ °C} = f(T_{hs})$

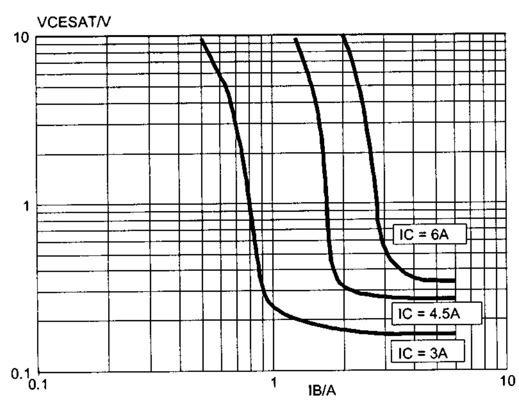


Fig. 9 Typical collector - emitter saturation voltage.
$V_{CE}sat = f(I_B)$; parameter I_C

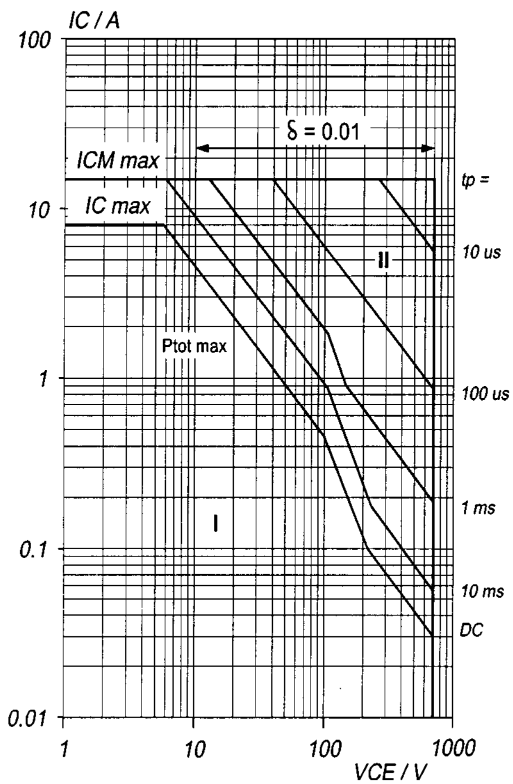


Fig. 12 Forward bias safe operating area. T_{hs} =25 °C
I Region of permissible DC operation
II Extension for repetitive pulse operation

NB: Mounted with heatsink compound and 30 ± 5 newton force on the centre of the envelope.

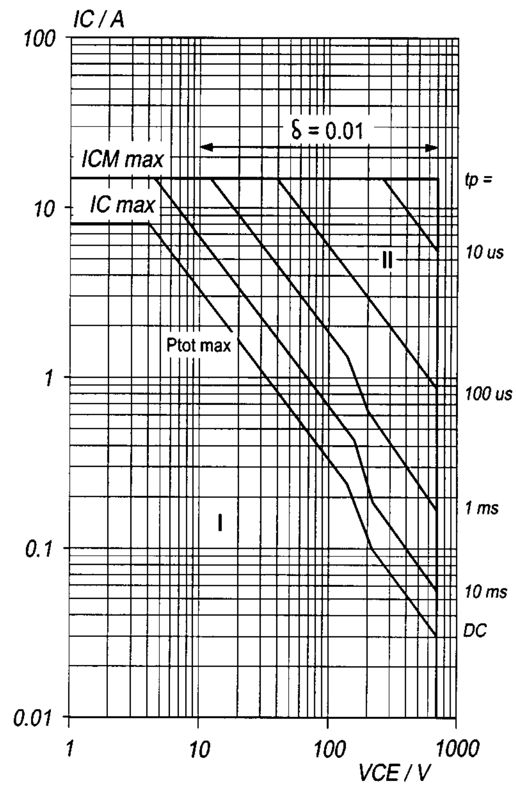


Fig. 13 Forward bias safe operating area. T_{hs} =25 °C
I Region of permissible DC operation
II Extension for repetitive pulse operation

NB: Mounted with heatsink compound and 30 ± 5 newton force on the centre of the envelope.

BU2525AF

Silicon Diffused Power Transistor

GENERAL DESCRIPTION

New generation, high voltage, high-speed switching npn transistor in a plastic full-pack envelope intended for use in horizontal deflection circuits of large screen colour television receivers up to 32 kHz.

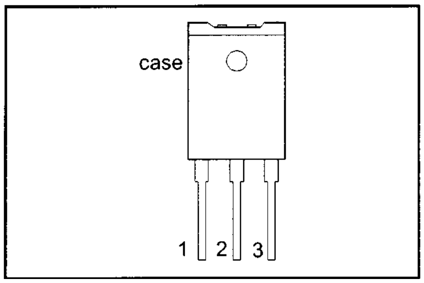
QUICK REFERENCE DATA

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	800	V
I_C	collector current (DC)		–	12	A
I_{CM}	collector current peak value		–	30	A
P_{tot}	total power dissipation	$T_{hs} \leq 25$ °C	–	45	W
V_{CEsat}	collector - emitter saturation voltage	I_C = 4.5 A; I_B = 1.6 A	–	5.0	V
I_{Csat}	collector saturation current	f = 16kHz	8.0	–	A
t_f	fall time	I_{csat} = 4.5 A; f = 16kHz	0.2	0.35	μs

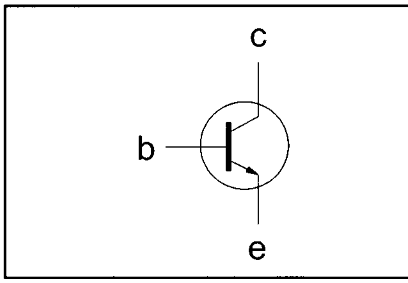
PINNING - SOT199

Pin	Description
1	base
2	collector
3	emitter
case	isolated

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134)

Symbol	Parameter	Conditions	Typ.	Max.	Unit
V_{CESM}	collector - emitter voltage peak value	V_{BE} = 0V	–	1500	V
V_{CEO}	collector - emitter voltage (open base)		–	800	V
I_C	collector current (DC)		–	12	A
I_{CM}	collector current peak value		–	30	A
I_B	Base current (DC)		–	8	A
I_{BM}	Base current peak value		–	12	mA
$-I_{B(AV)}$	Reverse base current	average over any 20 ms period	–	200	mA
$-I_{BM}$	Reverse base current peak value		–	7	mA
P_{tot}	Total power dissipation	$T_{hs} \leq 25$ °C	–	45	W
T_{stg}	Storage temperature		-65	150	°C
T_j	Junction temperature		–	150	°C

THERMAL RESISTANCES

Symbol	Parameter	Conditions	Typ.	Max.	Unit
$R_{th\ j-hs}$	Junction to heatsink	without heatsink compound	–	3.7	K/W
$R_{th\ j-hs}$	Junction to heatsink	with heatsink compound	–	2.8	K/W
$R_{th\ j-a}$	Junction to ambient	in free air	35	–	K/W

ISOLATION LIMITING VALUE & CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{isol}	Repetitive peak voltage from all three terminals to external heatsink	R.H.≤ 65%; clean and dustfree	–		2500	V
C_{isol}	Capaticance from T2 to external heatsink	f= 1 MHz	–	22	–	pF

STATIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{ces}	Collector cut-off current [2]	V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$	–	–	1.0	mA
I_{ces}		V_{BE} = 0 V; V_{CE} = $V_{CESMmax}$ [2] T_j = 125 °C	–	–	2.0	mA
I_{EBO}	Emitter cut-off current	V_{EB} = 7.5 V; I_C = 0A	–	–	1.0	mA
BV_{EBO}	Emitter -base breakdown voltage	I_B =1 mA	7.5	13.5	–	V
$V_{CEOsust}$	Collector-emitter sustaining voltage	I_B = 0A; I_c = 100 mA; L = 25 mH	800	–	–	V
V_{CEsat}	Collector-emitter saturation voltages	I_C = 8.0 A; I_B = 1.6 A;	–	–	5.0	V
V_{BEsat}	Base-emitter saturation voltages	I_C = 8.0 A; I_B = 1.6 A;	–	–	1.1	V
h_{FE}	DC current gain	I_C = 100 mA; V_{CE} = 5 V	–	13	–	
		I_C = 8 A; V_{CE} = 5 V	5	7	9.5	

DYNAMIC CHARACTERISTICS

T_{hs} = 25 °C; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
C_c	Collector capacitance	I_E = 0A; V_{CB} = 10V; f = 1 MHz	145	–	pF
	Switching times (32 kHz line deflection circuit)	I_{Csat} = 8.0 A; L_c= 260 μH; C_{fb} = 13 nF $I_{B(end)}$ + 1.1 A; L_B = 2.5 μH; -V_{BB} = 4 V; (-dI_B/dt= 1,6 A/μs)			
t_s	Turn-off storage time		3.0	4.0	μs
t_f	Turn-off fall time		0.2	0.35	μs

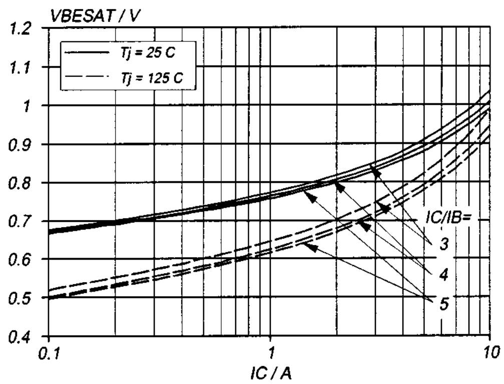


Fig. 7 Typical base-emitter saturation voltage.
$V_{BE}sat = f (I_c)$; parameter I_C/I_B

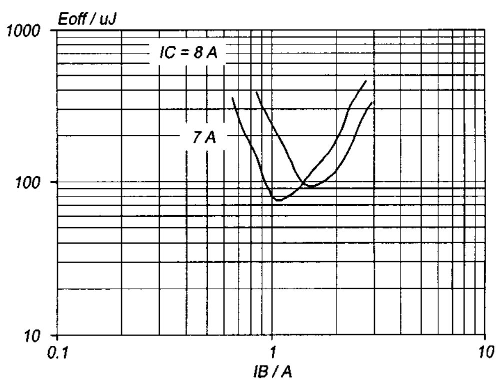


Fig. 8 Typical collector-emitter saturation voltage.
$V_{CE}sat = f (I_c)$; parameter I_C/I_B

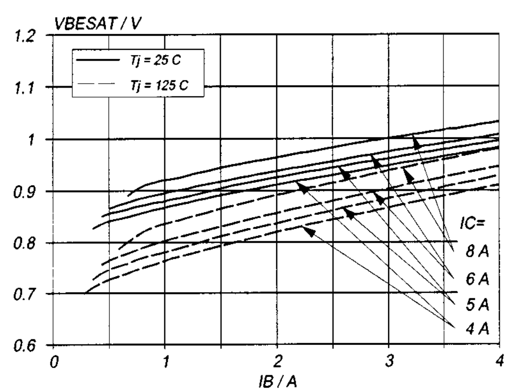


Fig. 9 Typical base-emitter saturation voltage.
$V_{BE}sat = f (I_B)$; parameter I_C

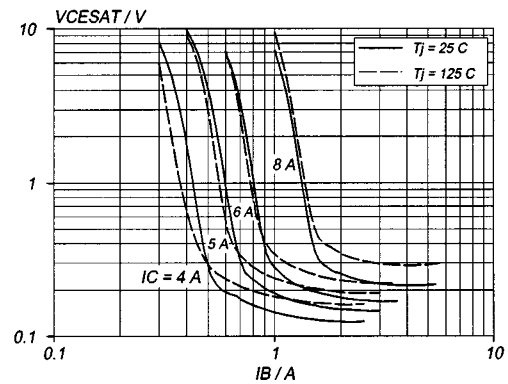


Fig. 10 Typical collector-emitter saturation voltage.
$V_{CE}sat = f (I_B)$; parameter I_C

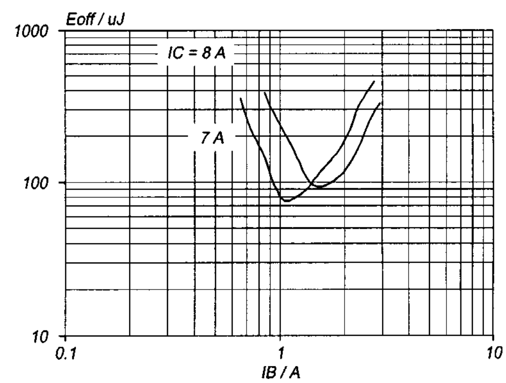


Fig. 11 Typical turn-off losses. $T_j = 85\ ^{\circ}C$
$E_{off} = f (I_B)$; parameter I_C; f = 32 kHz

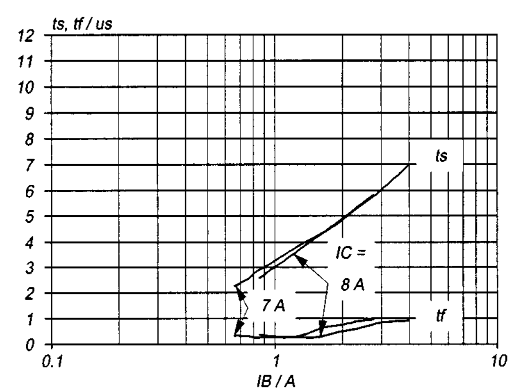


Fig. 12 Typical collector storage and fall time.
$ts = f (I_B)$; $tf = f (I_B)$; parameter I_C; $T_j = 85\ ^{\circ}C$; f = 32 kHz

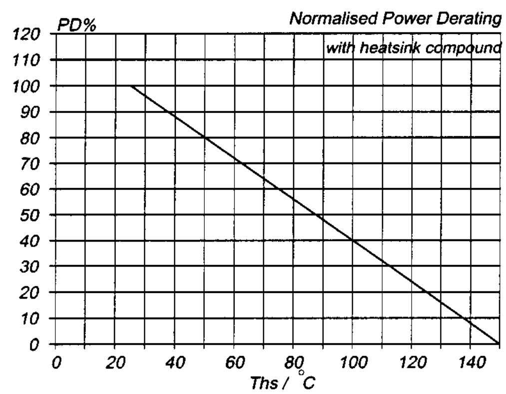


Fig. 13 Normalised power dissipation.
$PD\% = 100\ P_D/P_{D\ 25\ °C} = f\ (T_{hs})$

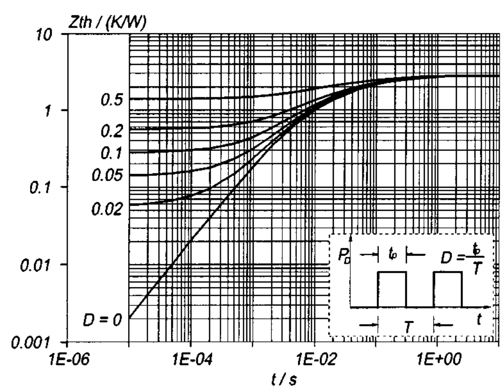


Fig. 14 Transient thermal impedance.
$Z_{th\ j\text{-}hs} = f\ (t)$; parameter $D = t_p/T$

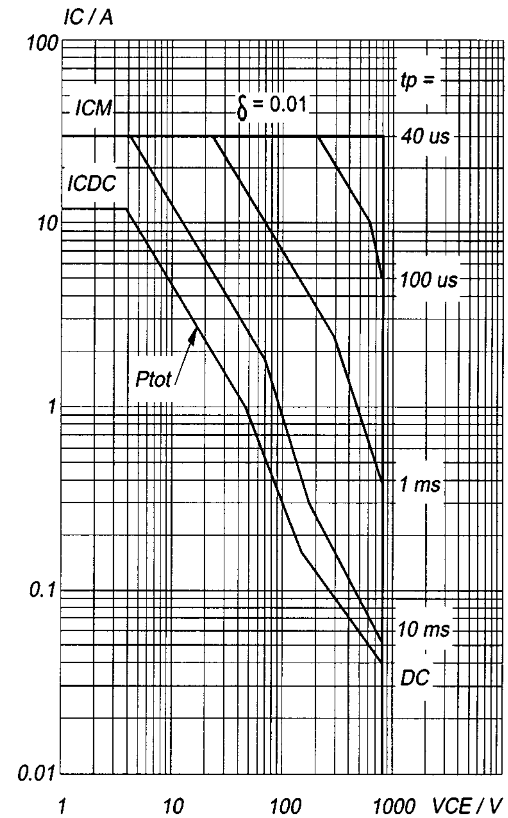
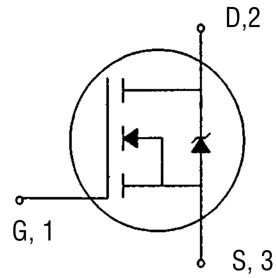
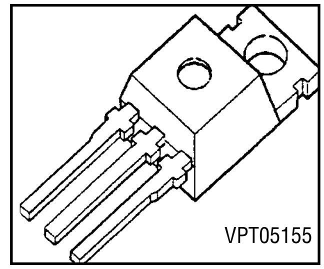


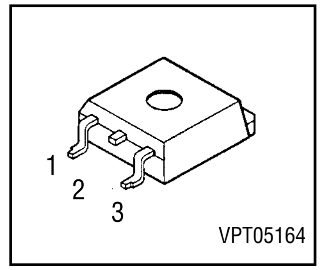
Fig. 15 Forward bias safe operating area. $T_{hs} = 25\ °C$
I_{CDC} & $I_{CM} = f(V_{CE})$; I_{CM} single pulse; parameter t_p
Second - breakdown limits independant of temperature.
Mounted with heatsink compound.

SPP04N60S5 / SPB04N60S5
Cool MOS Power Transistor

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche proved
- Extreme d_v/d_t rated
- Optimized capacitances
- Improved noise immunity
- Former development designation: SPPx6N60S5/SPBx6N60S5







Type	V_{DS}	I_D	$R_{DS(on)}$	Package	Marking	Ordering Code
SPP04N60S5	600V	4.5A	0.95Ω	P-TO220-3-1	04N60S5	Q67040-S4200
SPB04N60S5				P-TO263-3-2	04N60S5	Q67040-S4201

MAXIMUM RATINGS
at T_j = 25 °C; unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C T_C = 100 °C	I_D	 4.5 2.8	A
Pulsed drain current, tp = 1ms (1) T_C = 25 °C	$I_{D\ puls}$	7.7	
Avalanche energy, single pulse I_D = 4.5A, V_{DD} = 50V, R_{GS} = 25Ω Periodic avalanche energy E_{AR} only limited by T_{jmax}	E_{AS}	130	mJ
Reverse diode d_v/d_t I_S = 4.5 A, $V_{DS}<V_{DSS}$, d_i/d_t = 100 A/µs, T_{jmax} = 150 °C	d_v/d_t	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_C = 25 °C	P_{tot}	50	W
Operating and storage temperature	T_j, T_{stg}	-55 ...+150	°C

ELECTRICAL CHARACTERISTICS

Parameter at T_j = 25 °C; unless otherwise specified	Symbol	Value min.	Value typ.	Value max.	Unit

Thermal Characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Thermal resistance, junction - case	R_{thJC}	–	–	2.5	K/W
Thermal resistance, junction - ambient (Leaded and through-hole packages)	R_{thJA}	–	–	62	
SMD version, device on PCB @ min. footprint @ 6 cm^2 cooling area [2]	RthJA	 – –	 – 35	 62 –	

Static Characteristics

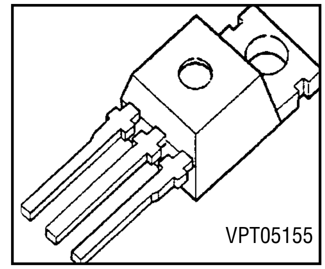
Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	–	–	V
Gate threshold voltage, $V_{GS} = V_{DS}$ I_D = 200 µA, T_j = 25 °C	$V_{GS(th)}$	3.5	4.5	5.5	
Zero gate voltage drain current, $V_{DS} = V_{DSS}$ V_{GS} = 0V, T_j = 25 °C V_{GS} = 0V, T_j = 150 °C	I_{DSS}	 – –	 0.5 –	 1 50	µA
Gate-source leakage current V_{GS} = 20V, V_{DS} = 0V	I_{GSS}	–	–	100	nA
Drain Source on-state resistance V_{GS} = 10V, I_D = 2.8A	$R_{DS(on)}$	–	0.85	0.95	Ω

[1] current limited by T_{jmax}

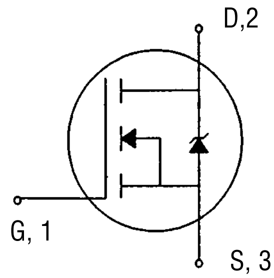
[2] Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

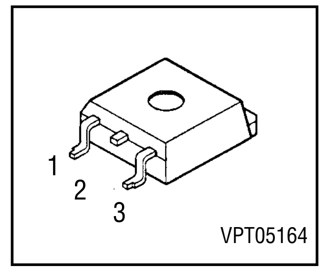
SPP07N60S5 / SPB07N60S5

Cool MOS Power Transistor



- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche proved
- Extreme d_v/d_t rated
- Optimized capacitances
- Improved noise immunity
- Former development designation:
  SPPx6N60S5/SPBx6N60S5





Type	V_{DS}	I_D	$R_{DS(on)}$	Package	Marking	Ordering Code
SPP07N60S5	600V	7.3A	0.6Ω	P-TO220-3-1	07N60S5	Q67040-S4172
SPB07N60S5				P-TO263-3-2	07N60S5	Q67040-S4185

MAXIMUM RATINGS

at T_j = 25 °C; unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current T_C = 25 °C T_C = 100 °C	I_D	 7.3 4.6	A
Pulsed drain current, tp = 1ms [(1)] T_C = 25 °C	$I_{D\ puls}$	14.6	
Avalanche energy, single pulse I_D = 7.3A, V_{DD} = 50V, R_{GS} = 25Ω Periodic avalanche energy E_{AR} only limited by T_{jmax}	E_{AS}	230	mJ
Reverse diode d_v/d_t I_S = 7.3 A, $V_{DS}<V_{DSS}$, d_i/d_t = 100 A/µs, T_{jmax} = 150 °C	d_v/d_t	6	kV/µs
Gate source voltage	V_{GS}	±20	V
Power dissipation T_C = 25 °C	P_{tot}	83	W
Operating and storage temperature	T_j, T_{stg}	-55 ...+150	°C

ELECTRICAL CHARACTERISTICS

Parameter at T_j = 25 °C; unless otherwise specified	**Symbol**	**Value** min.	typ.	max.	**Unit**

Thermal Characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Thermal resistance, junction - case	R_{thJC}	–	–	1.5	K/W
Thermal resistance, junction - ambient (Leaded and through-hole packages)	R_{thJA}	–	–	62	
SMD version, device on PCB @ min. footprint @ 6 cm^2 cooling area [(2)]	RthJA	 – –	 – 35	 62 –	

Static Characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Drain-source breakdown voltage V_{GS} = 0V, I_D = 0.25 mA	$V_{(BR)DSS}$	600	–	–	V
Gate threshold voltage, $V_{GS} = V_{DS}$ I_D = 350 µA, T_j = 25 °C	$V_{GS(th)}$	3.5	4.5	5.5	
Zero gate voltage drain current, $V_{DS} = V_{DSS}$ V_{GS} = 0V, T_j = 25 °C V_{GS} = 0V, T_j = 150 °C	I_{DSS}	 – –	 0.5 –	 1 100	µA
Gate-source leakage current V_{GS} = 20V, V_{DS} = 0V	I_{GSS}	–	–	100	nA
Drain Source on-state resistance V_{GS} = 10V, I_D = 4.6A	$R_{DS(on)}$	–	0.85	0.95	Ω

1 current limited by T_{jmax}

2 Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

ELECTRICAL CHARACTERISTICS

Parameter at T_j = 25 °C; unless otherwise specified	Symbol	Value min.	Value typ.	Value max.	Unit

Characteristics

Parameter	Symbol	min.	typ.	max.	Unit
Transconductance $V_{DS} \geq 2 * I_D * R_{DS(on)max}$, I_D = 4.6 A	g_{fs}	–	4	–	S
Input capacitance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{iss}	–	970	–	pF
Output capaticance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	Coss	–	510	–	
Reverse transfer capaticance V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	C_{rss}	–	17	–	
Turn-on delay time V_{DD} = 350 V, V_{GS} = 10 V, I_D = 7.3 A R_G = 12 Ω	Td(on)	–	45	–	ns
RİSE time V_{DD} = 350 V, V_{GS} = 10 V, I_D = 7.3 A R_G = 12 Ω	TR	–	30	–	
Turn-off delay time V_{DD} = 350 V, V_{GS} = 10 V, I_D = 7.3 A R_G = 12 Ω	Td(off)	–	70	–	
Fall time V_{DD} = 350 V, V_{GS} = 10 V, I_D = 7.3 A R_G = 12 Ω	Tf	–	30	–	

ELECTRICAL CHARACTERISTICS

Parameter at T_j = 25 °C; unless otherwise specified	Symbol	Value			Unit
		min.	typ.	max.	

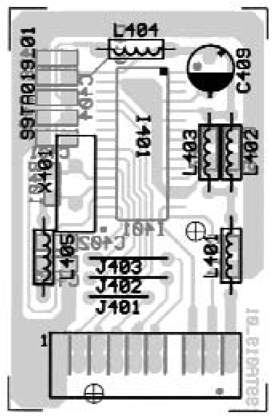
Gate Charge Characteristics

Gate-source charge I_D = 7.3 A, V_{DD} = 350 V	Q_{gs}	–	6.7	–	nC
Gate-drain charge I_D = 7.3 A, V_{DD} = 350 V	Q_{gd}	–	15.3	–	
Total gate charge I_D = 7.3 A, V_{DD} = 350 V, V_{GS} = 0 to 10 V	Q_g	–	27	–	

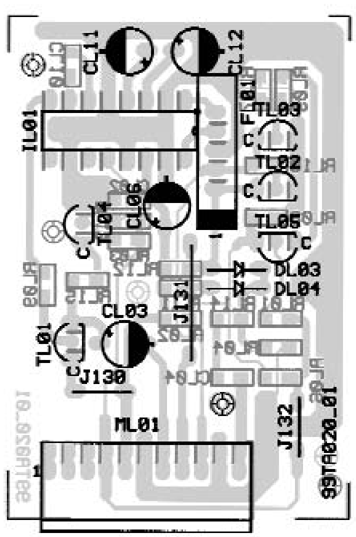
Reverse Diode

Inverse diode continuous forward current T_C = 25 °C	I_S	–	–	7.3	A
Inverse diode direct current, pulsed T_C = 25 °C	I_{SM}	–	–	14.6	
Inverse diode forward voltage V_{GS} = 0 V, I_F = 7.3 A	V_{SD}	–	1	1.2	V
Reverse recovery time V_R = 350 V, $I_F = I_S$, di_F/dt = 100 A/µs	t_{rr}	–	750	–	ns
Reverse recovery charge V_R = 350 V, $I_F = I_S$, di_F/dt = 100 A/µs	Q_{rr}	–	4.9	–	µC

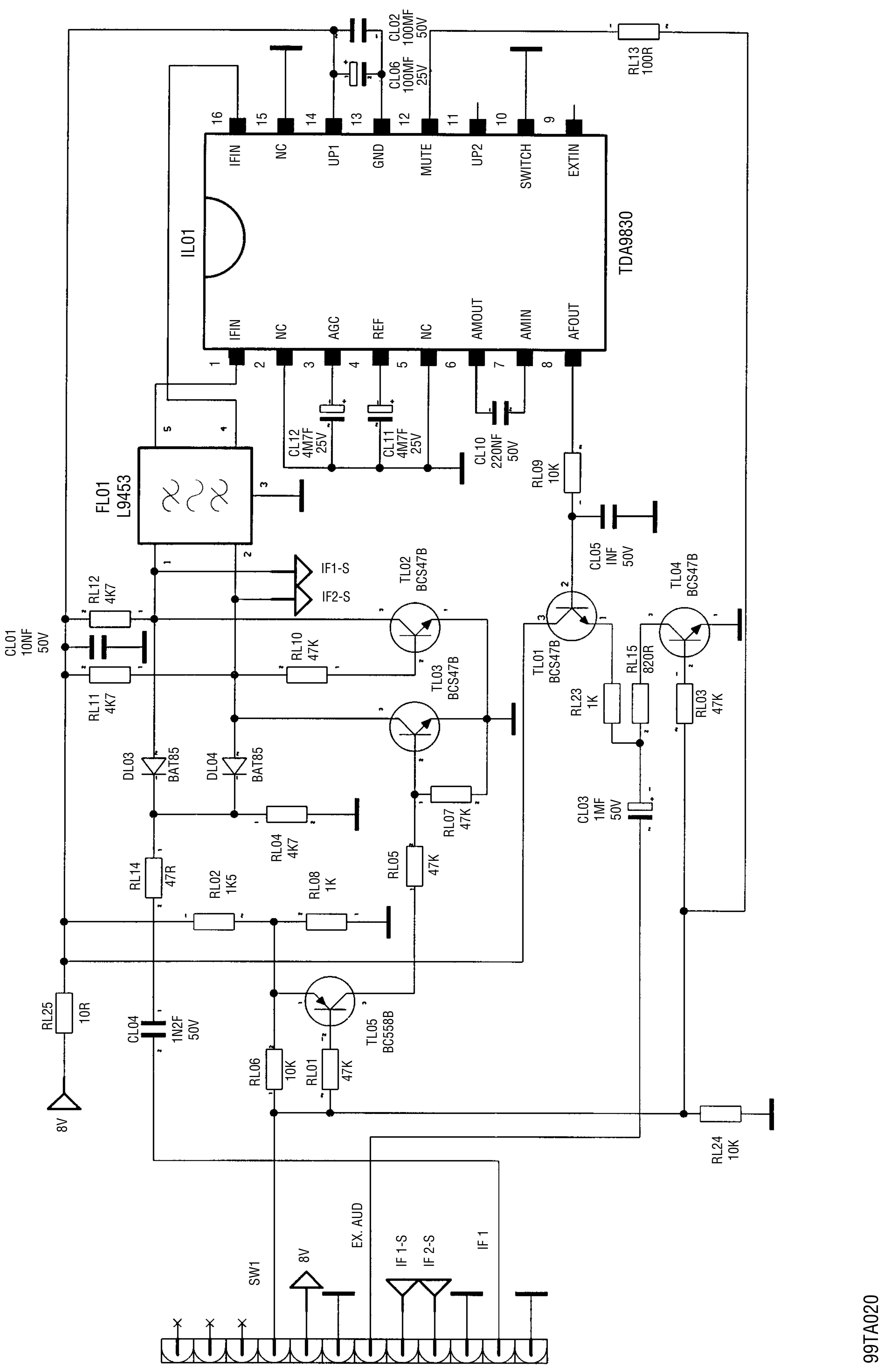
PT-92 DOLBY BOARD



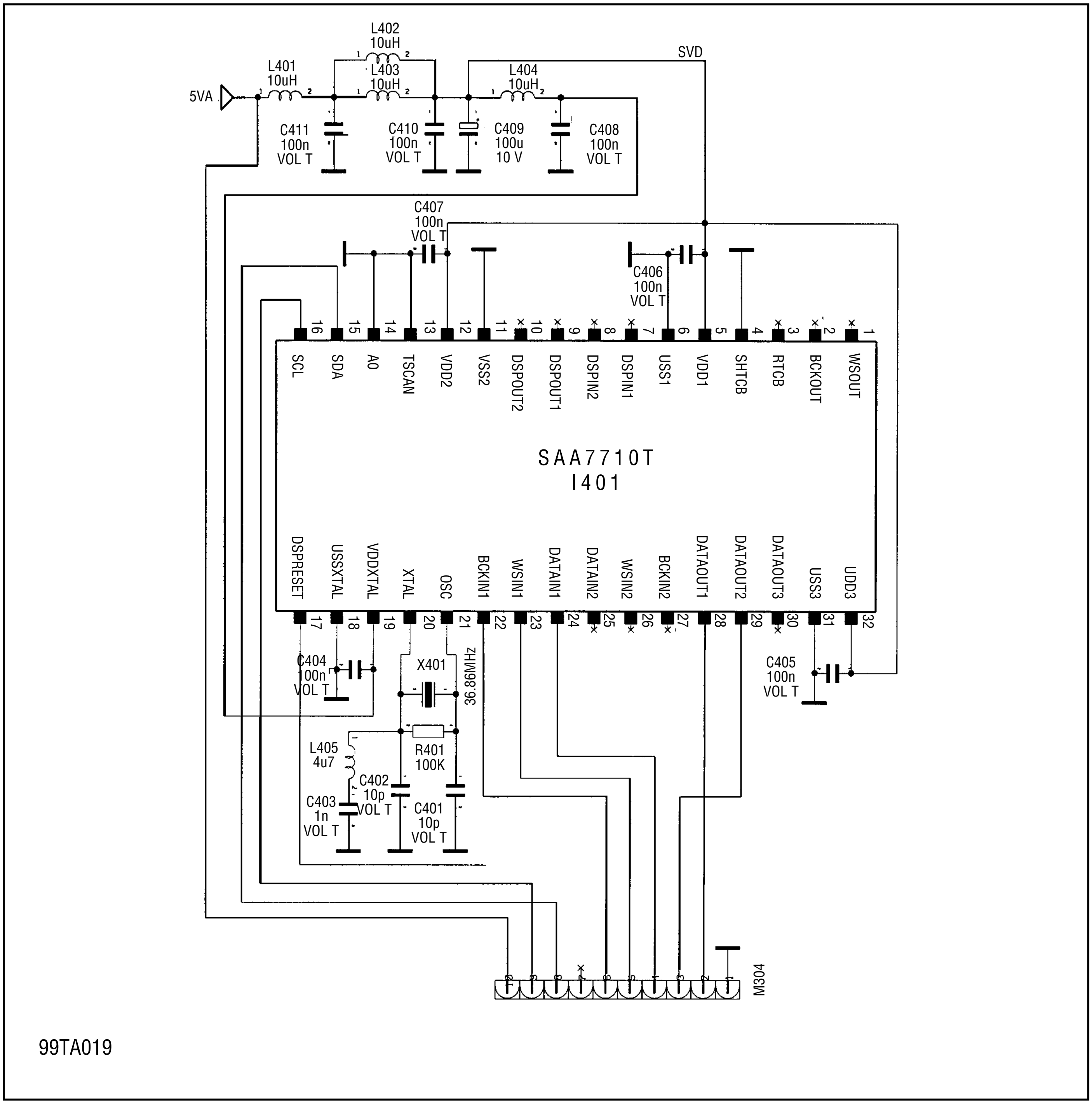
PT-92 SECAM L



PT-92 SECAM L/L' MONO MODUL

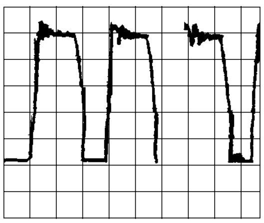


PT-92 DOLBY MODUL



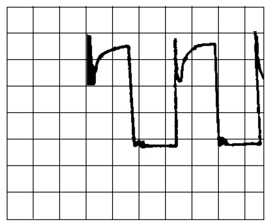
OSCILLOSCOPE SHAPES

1) 5usn/div 100 volt/div



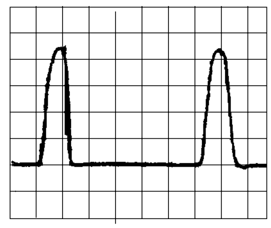
Drain of TP01

2) 20msn/50 volts/div



Collector of TD01

3) 10 usn/div 250 volt/div



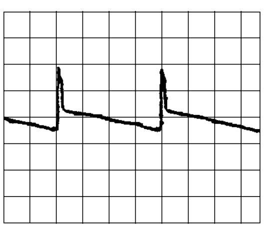
Collector of TD02

4) 5 msn/div 0.5 volt/div



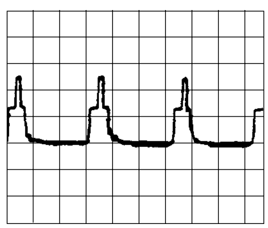
I V01 pin 22

5) 5msn/div 20 volts/div



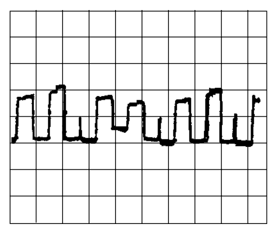
I D50 pin 4

6) 20usn/2 volts/div



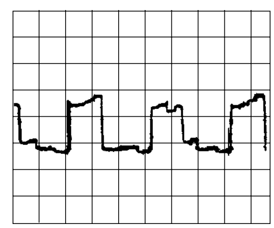
I V01 pin 34

7) 20usn/2 volts/div



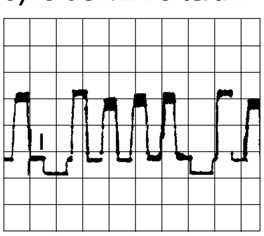
I V01 pin 48

8) 20usn/2 volts/div



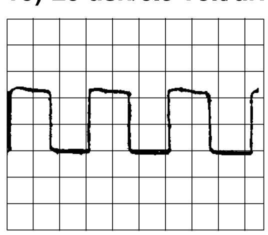
I V01 pin 47

9)10 usn/2 volts/div



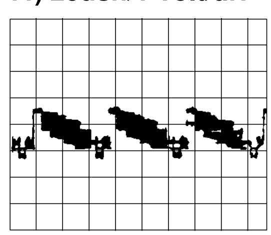
I V01 pin 46

10) 20 usn/0.5 volt/div



I V01 pin 33

11) 20usn/1 volt/div



I V01 pin 40